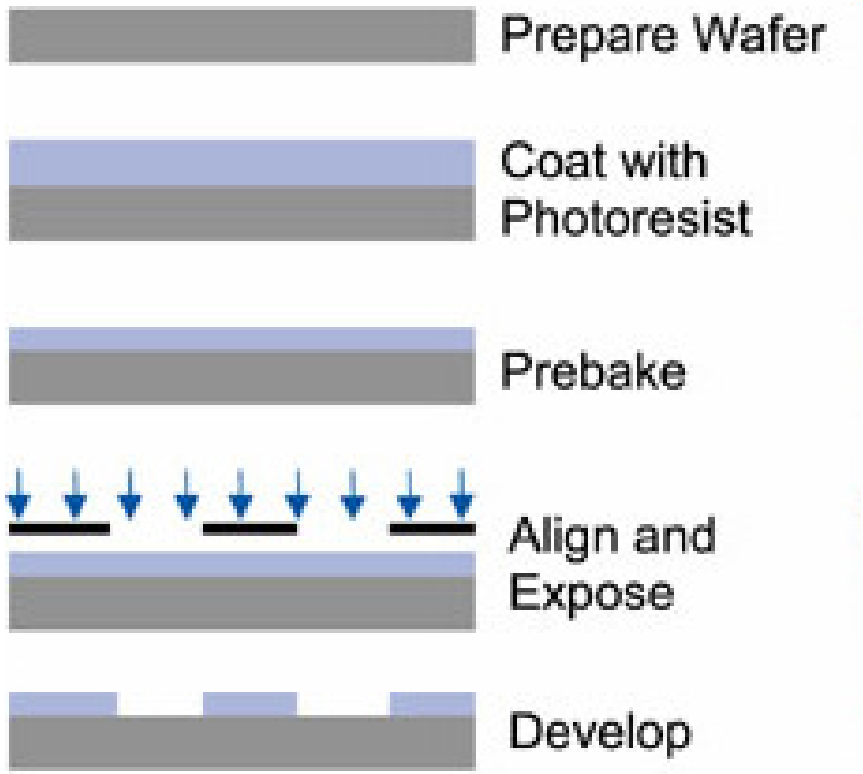
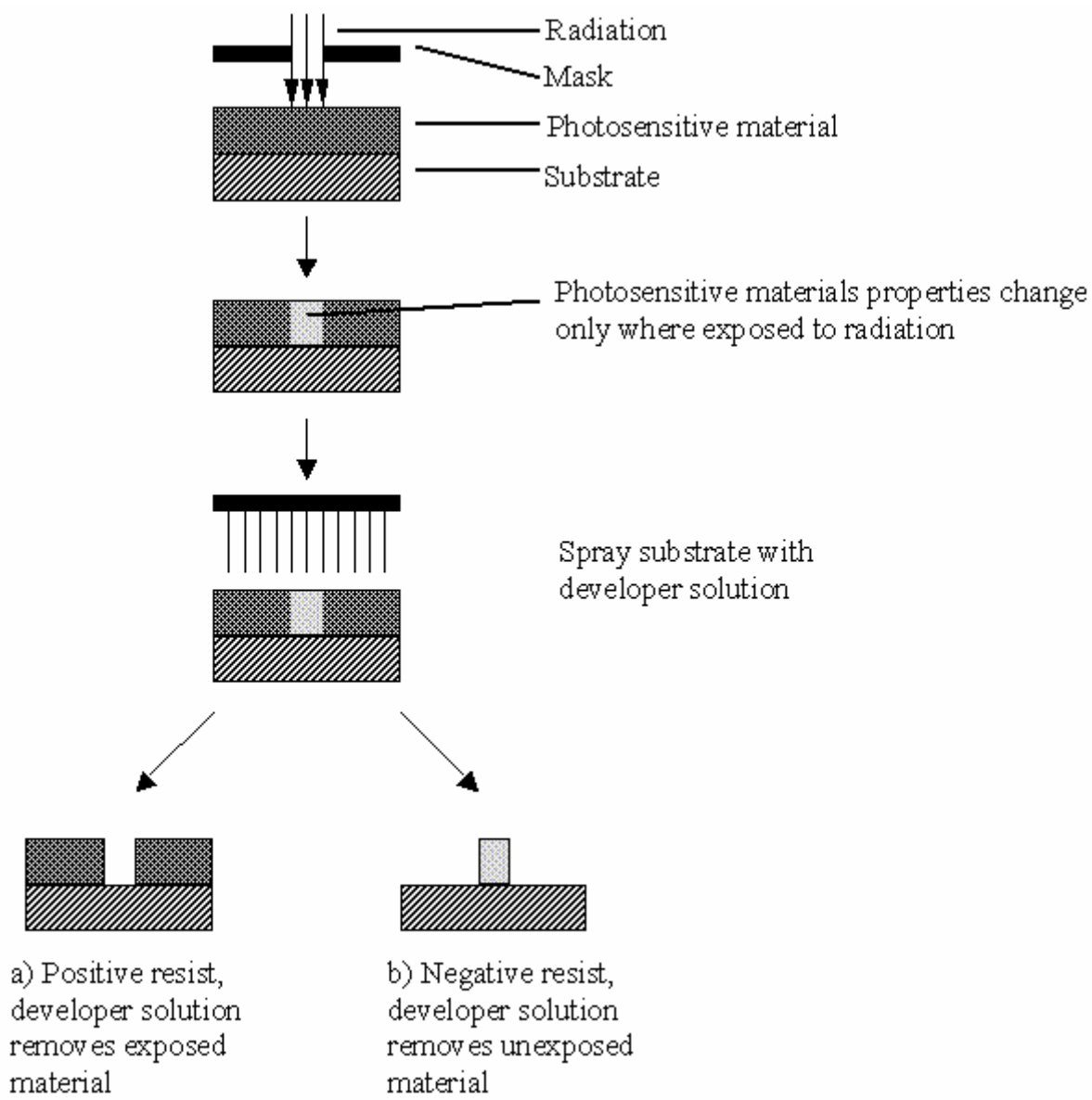
Litografia


Prepare Wafer
Coat with
Photoresist
Prebake
Align and
Expose
Develop

Litografia


Radiation
Mask
Photosensitive material
Substrate
Photosensitive materials properties change only where exposed to radiation
Spray substrate with developer solution
a) Positive resist, developer solution removes exposed material
b) Negative resist, developer solution removes unexposed material

Litografia

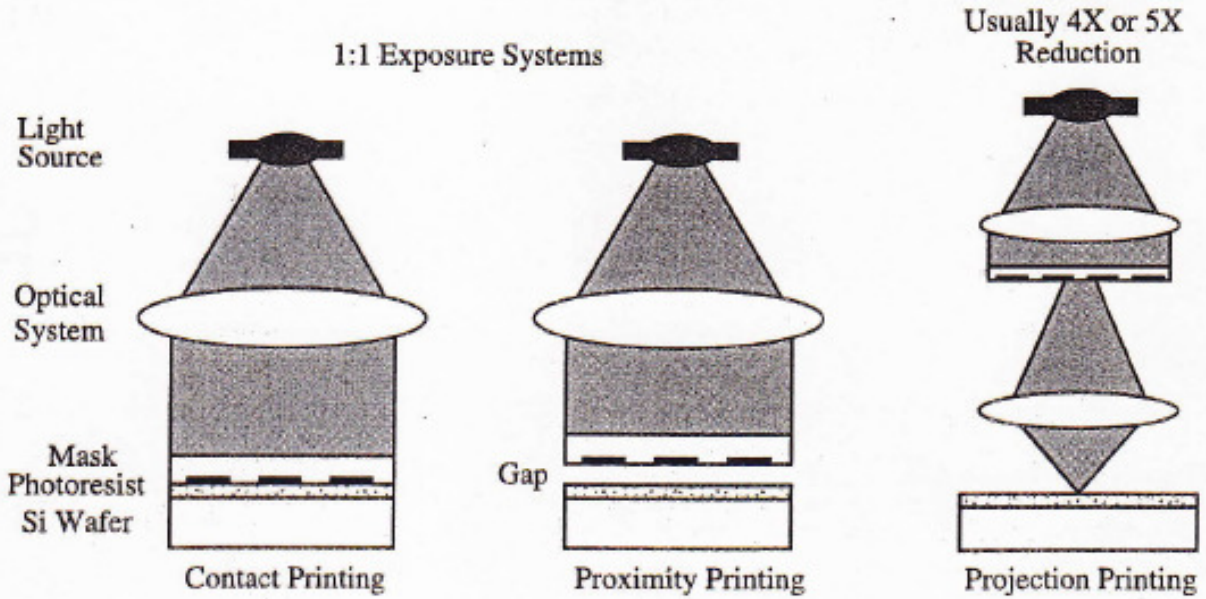
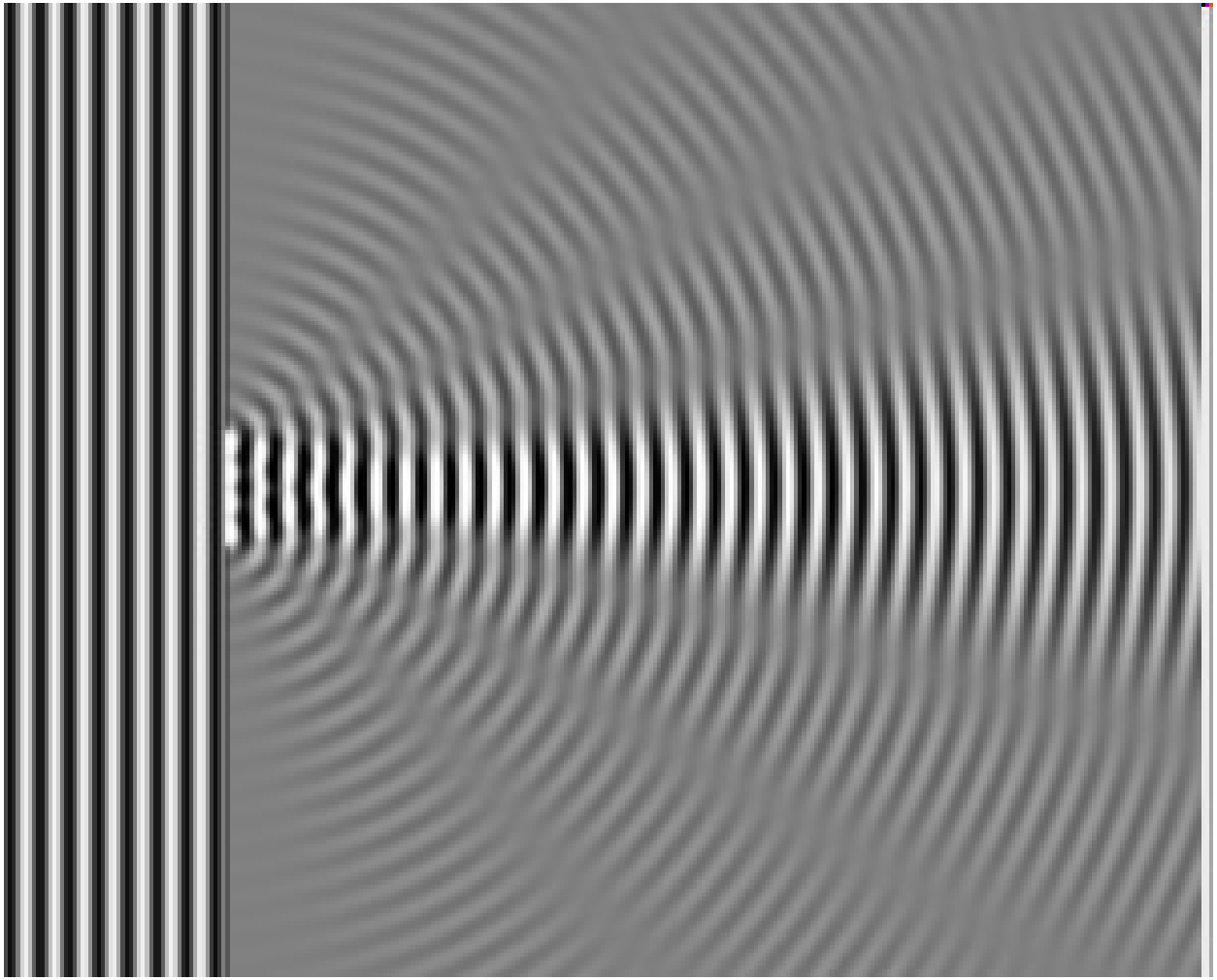
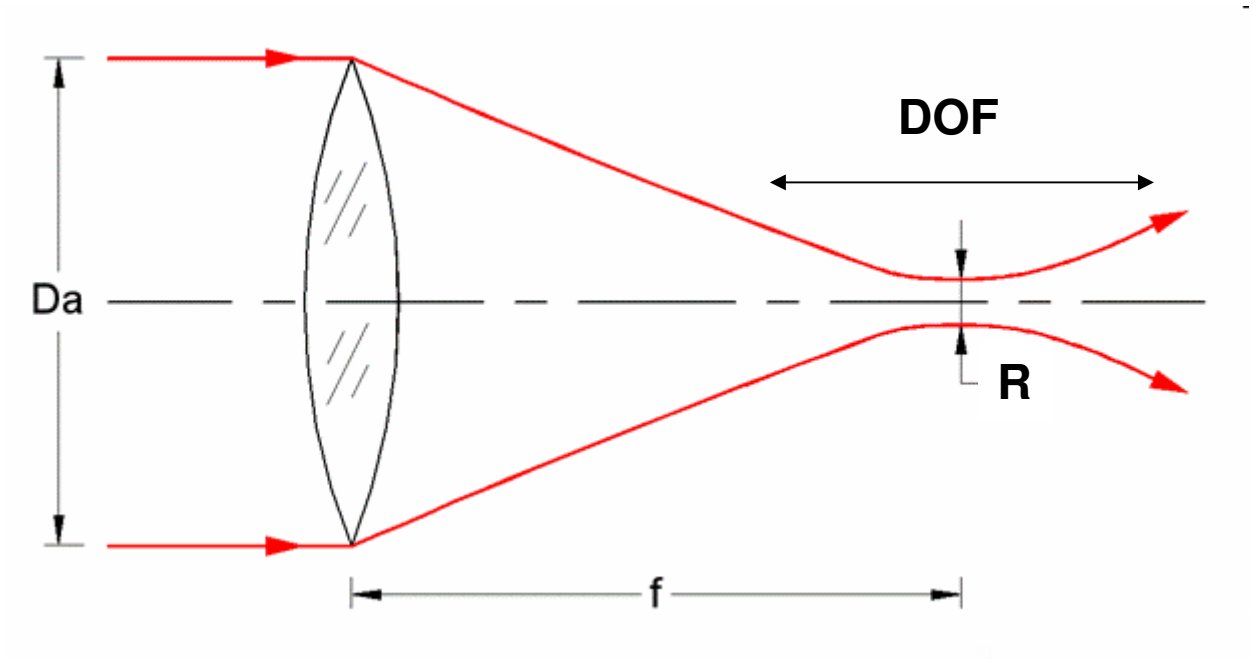


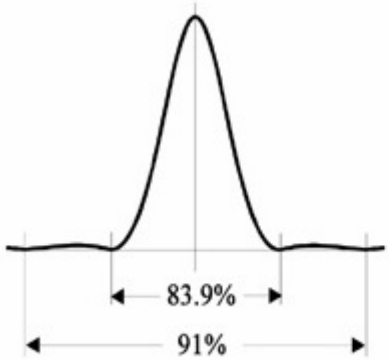
Figure 5–3 Three basic methods of wafer exposure.

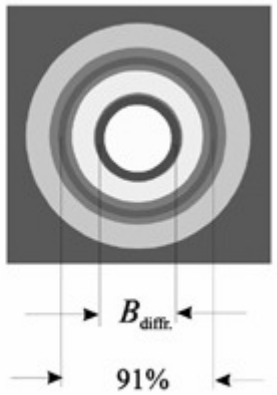
Diffrazione



Limite diffrattivo







Limits of optical lithography ?

- **Rayleigh criteria** :

$$R = k_1 \times \frac{\lambda}{NA} \quad with \quad NA = n \times \sin(\theta) < n$$

$$DOF = k_2 \frac{\lambda}{NA^2}$$

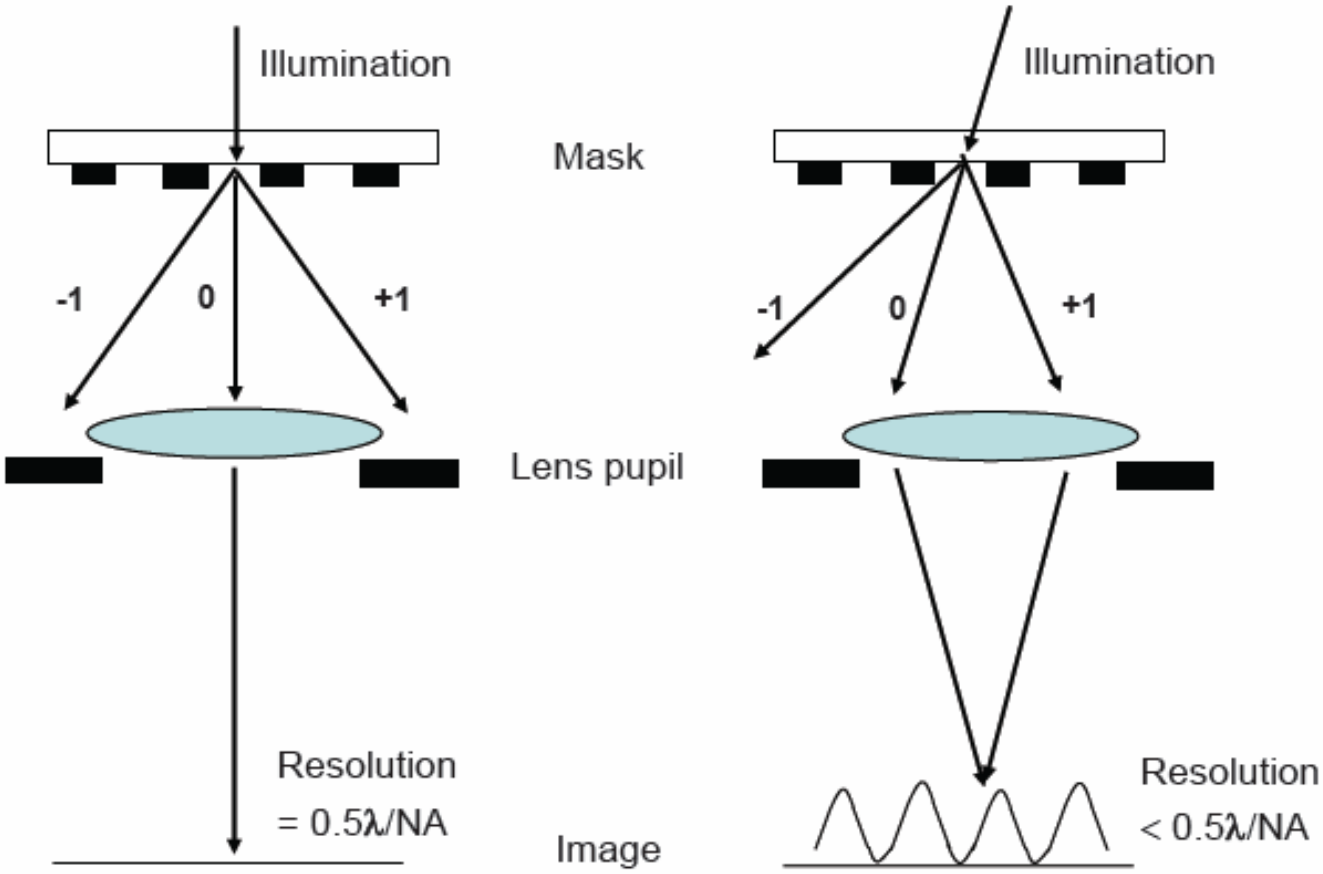
➔To improve resolution we need to:

➔Decrease k1
➔Increase NA
➔Decrease λ

- **k_1 decrease is made through:**
  - Resist improvement
  - OPC and PSM masks
  - Off axis illumination or polarization

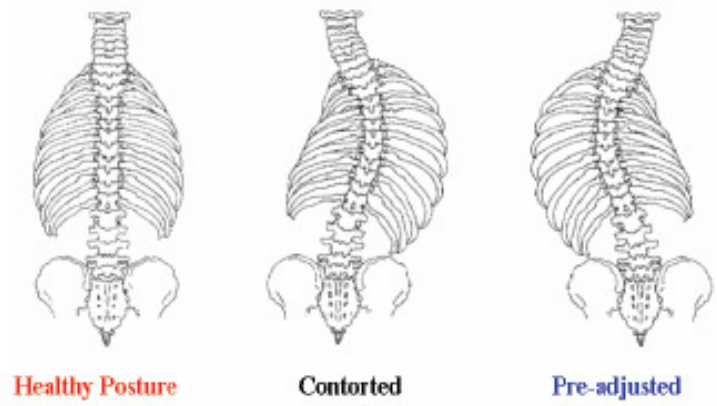
Off-Axis Illumination (OAI)

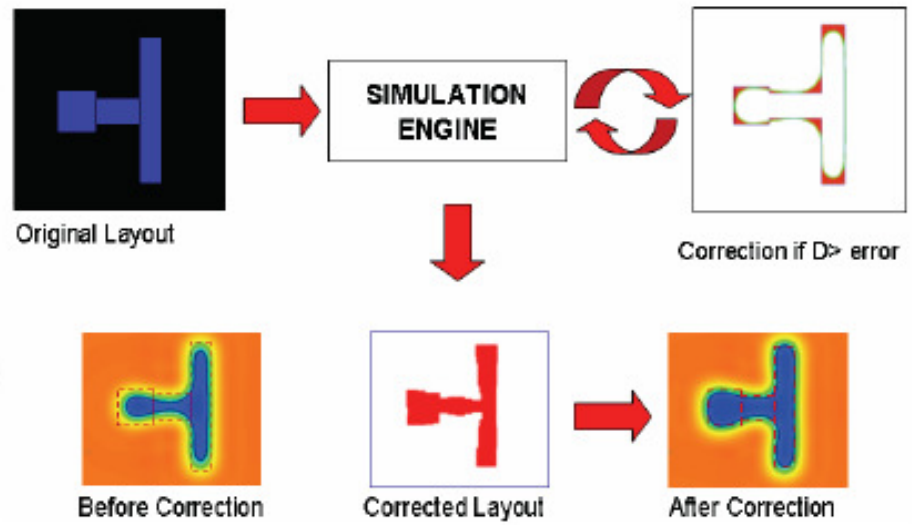
- Primarily used for improving resolution/DOF of dense features



Optical Proximity Correction (OPC)

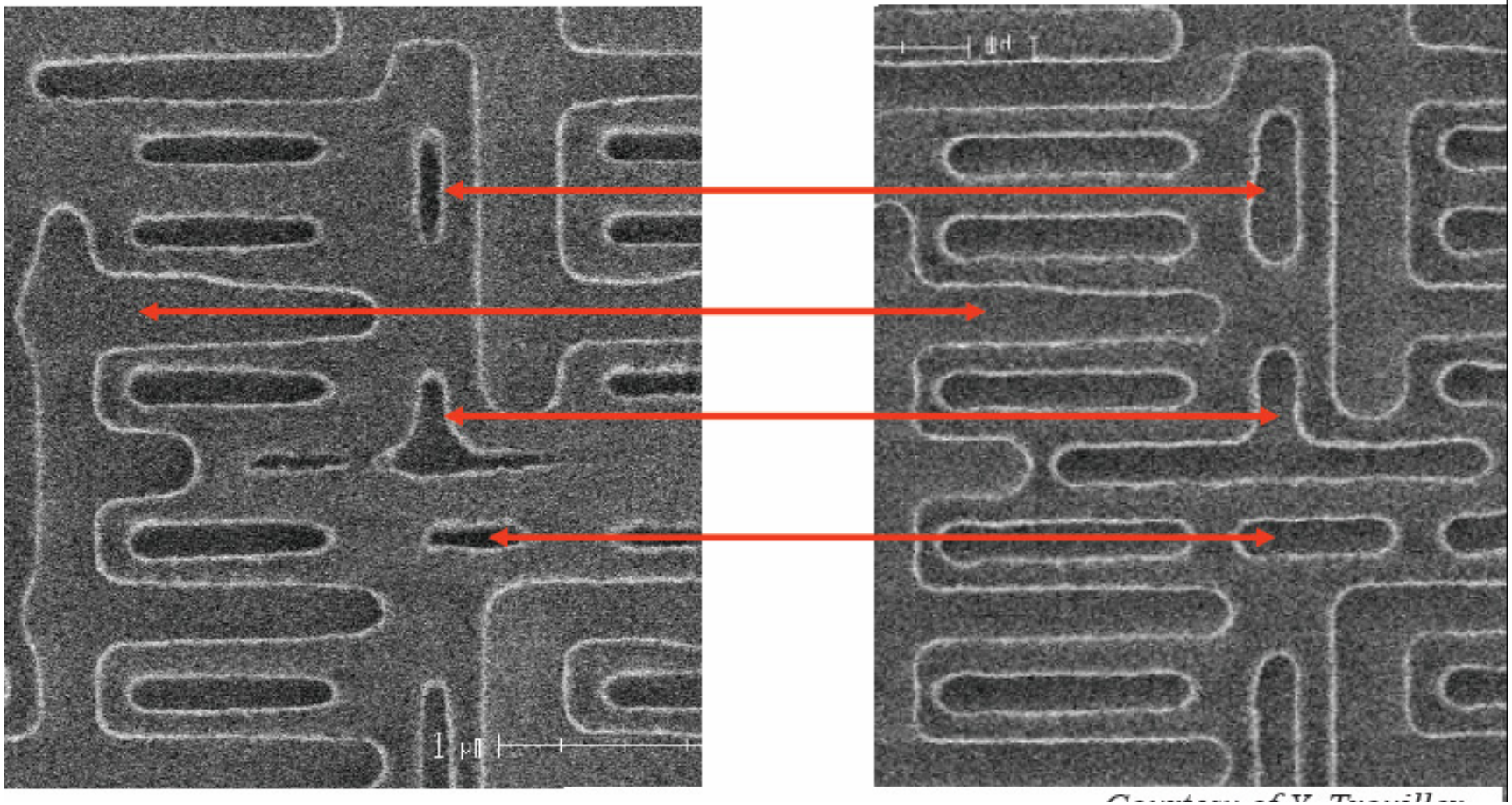
OPC : precorrect the mask to have the silicon result as close as possible to the original design





Optical Proximity Correction (OPC)

No OPC C065 Metal1 OPC

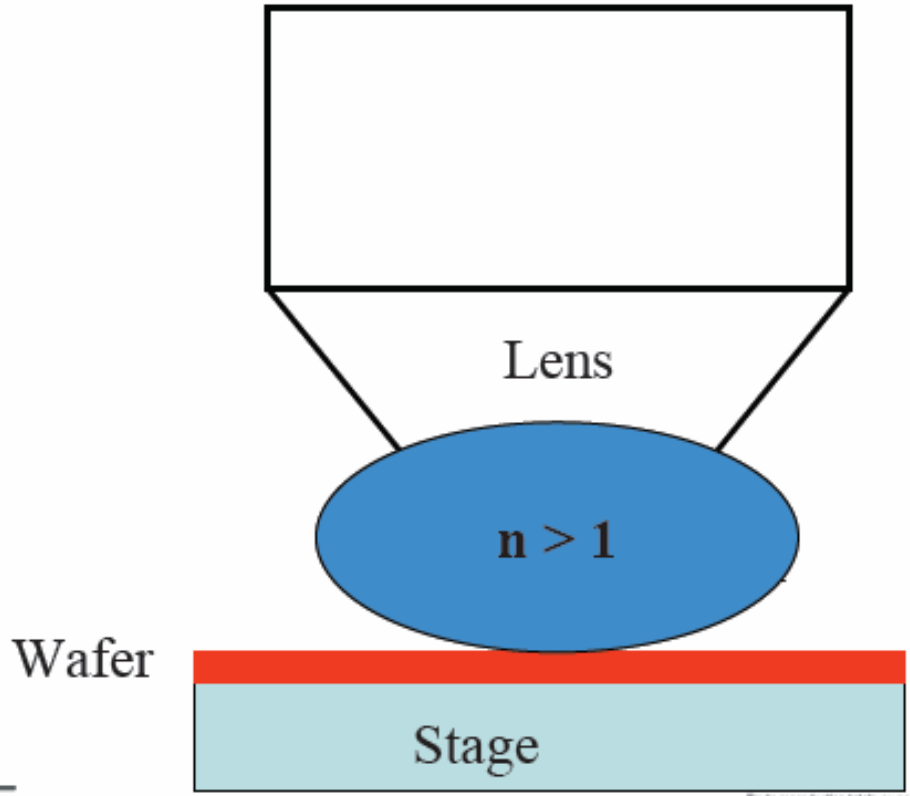


Courtesy of K. Tsuneiller

Numerical Aperture increase

- In air max achievable NA is 1
- Today state of the art dry system achieve NA =0.93

Introduction of immersion lithography allows to reach NA >1



$$NA = n \sin \theta$$

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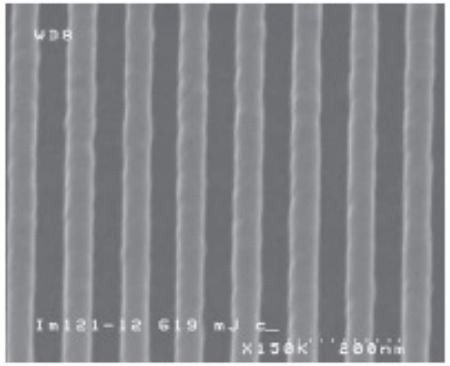
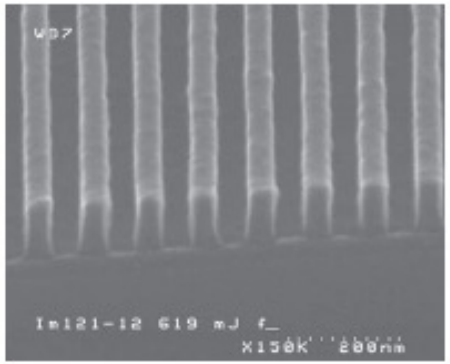
Immersion lithography with water

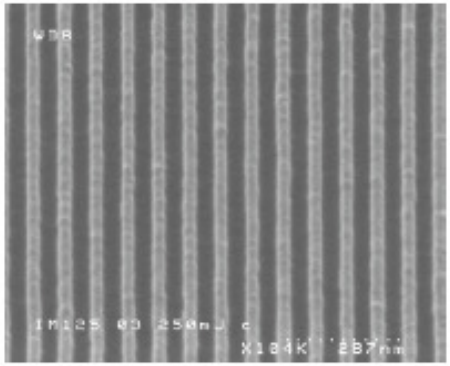
55 nm hp imaging NA=0.87

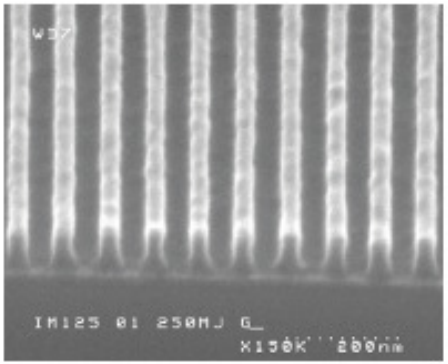




CD = 47 nm

40 nm hp imaging NA=1.2

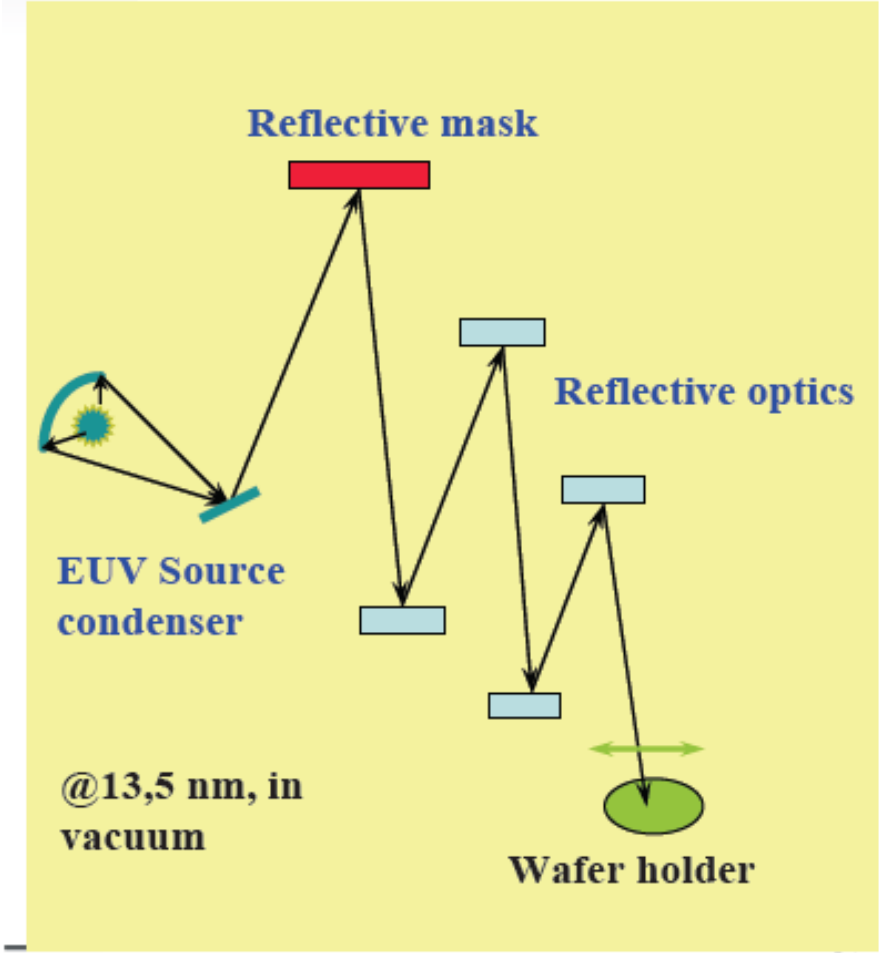




CD = 39 nm

EUV Lithograpy: technological breakthrough

The big jump from DUV 193 nm to EUV 13.5 nm



Everything absorb EUV light

- ✓Vacuum
- ✓Reflective masks and optics

Sources: based on plasma (Xe,Sn,In) emitting in EUV (13.5 nm)

- ✓Laser Produce Plasma (LPP)
- ✓Discharge Produce Plasma (DPP)

Specifications very tight

- ✓ML mirrors: 70% reflectivity
- ✓Masks: defects < 10^{-3} defects/cm2
- ✓optics: < 0.1 nm roughness
- ✓sources: 180 W, no debris

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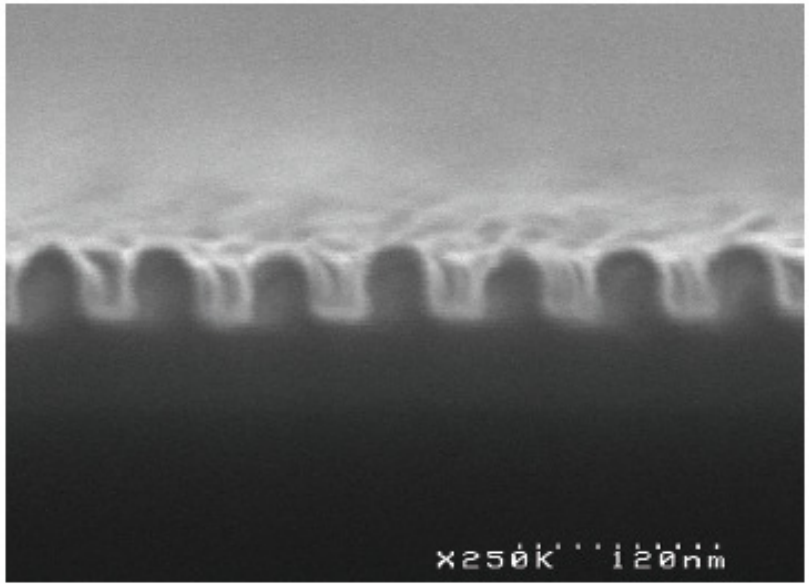
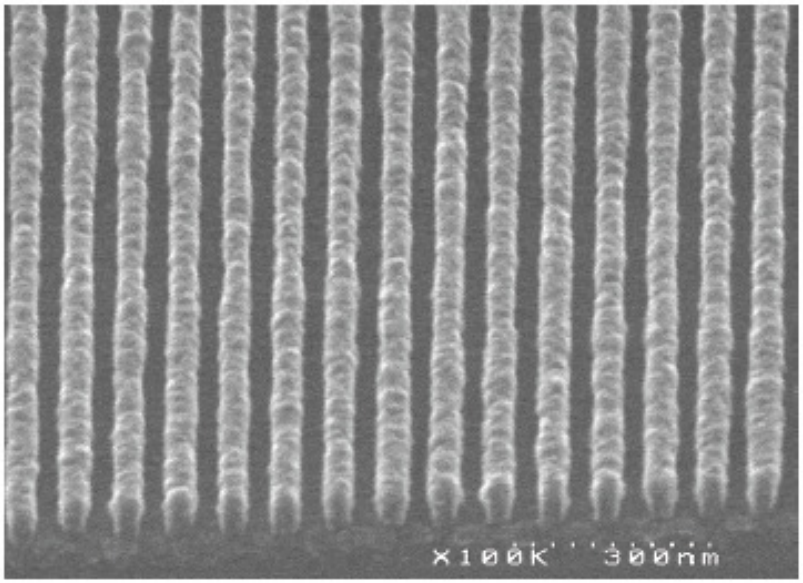
EUV lithography main achievements





32.5 nm L/S on CAR using IL-EUV at PSI

ASML technology roadmap scenarios

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

Pitch relaxation or Double patterning

Low k_1 challenge

Fluid/ material challenge

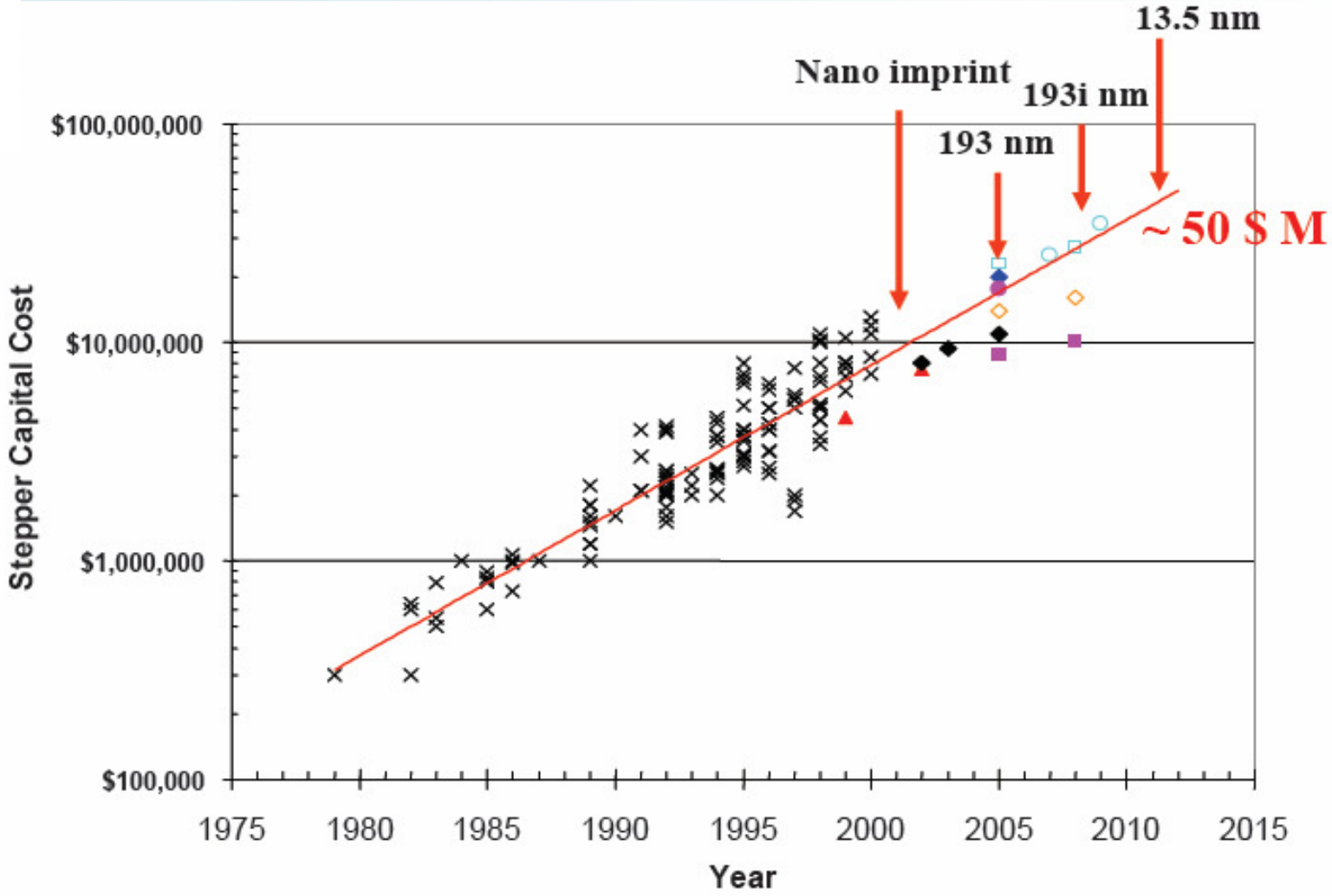
Infrastructure challenge

likely

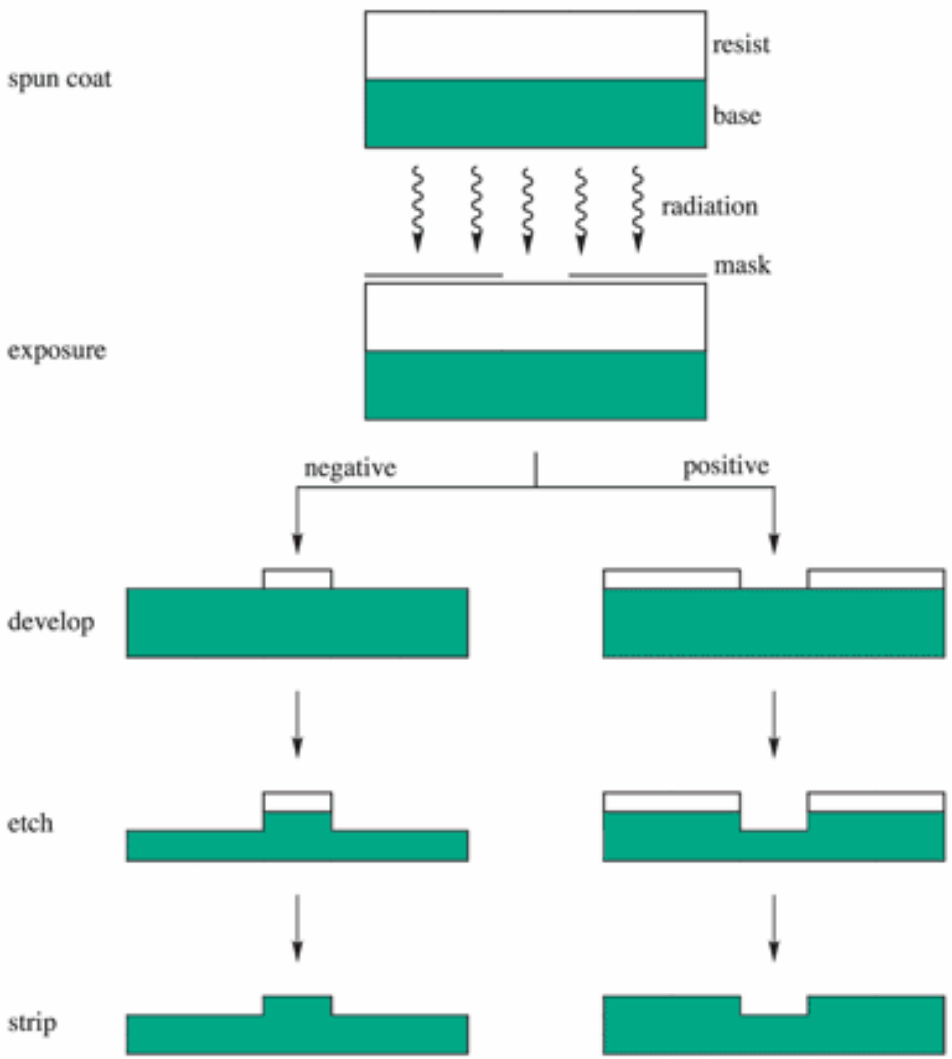
opportunity

ASML

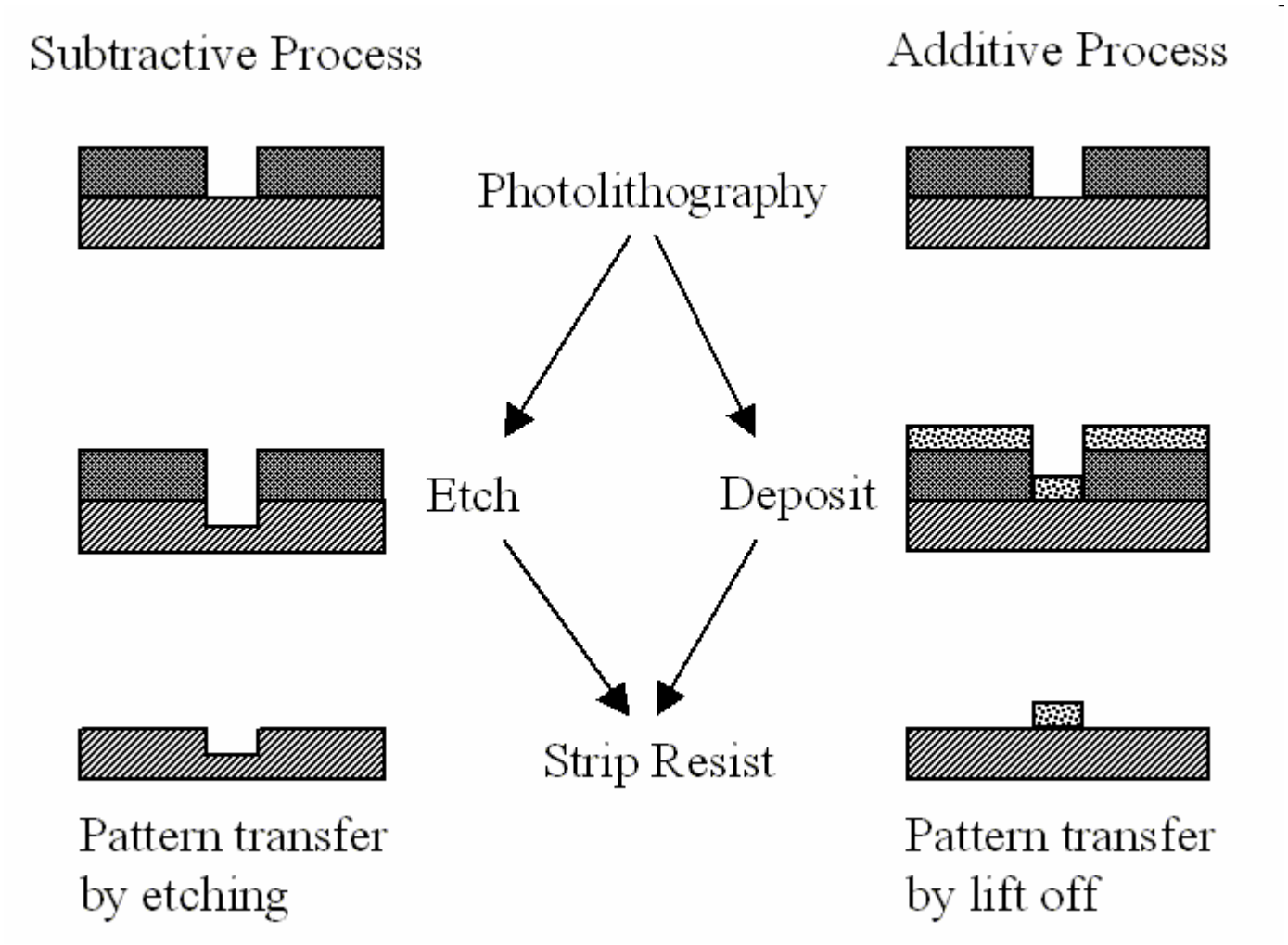
Equipment cost



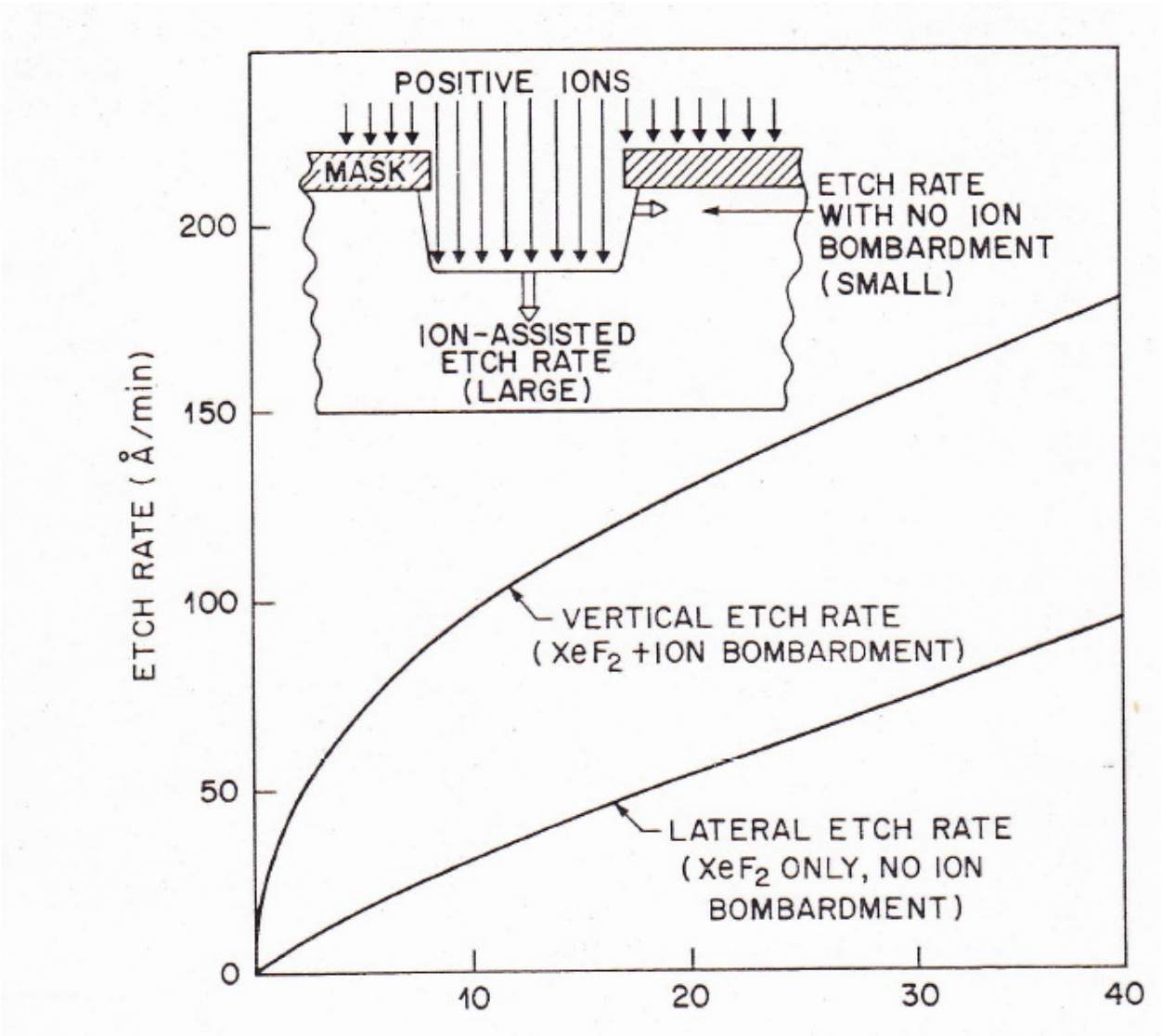
Etching


spun coat
resist
base
radiation
mask
exposure
negative
positive
develop
etch
strip

Etching and/or deposition



Dry Etching


POSITIVE IONS
MASK
ETCH RATE WITH NO ION BOMBARDMENT (SMALL)
ION-ASSISTED ETCH RATE (LARGE)
ETCH RATE (Å/min)
200
150
100
50
0
10
20
30
40
VERTICAL ETCH RATE (XeF_2 +ION BOMBARDMENT)
LATERAL ETCH RATE (XeF_2 ONLY, NO ION BOMBARDMENT)

Costruzione MOSFET

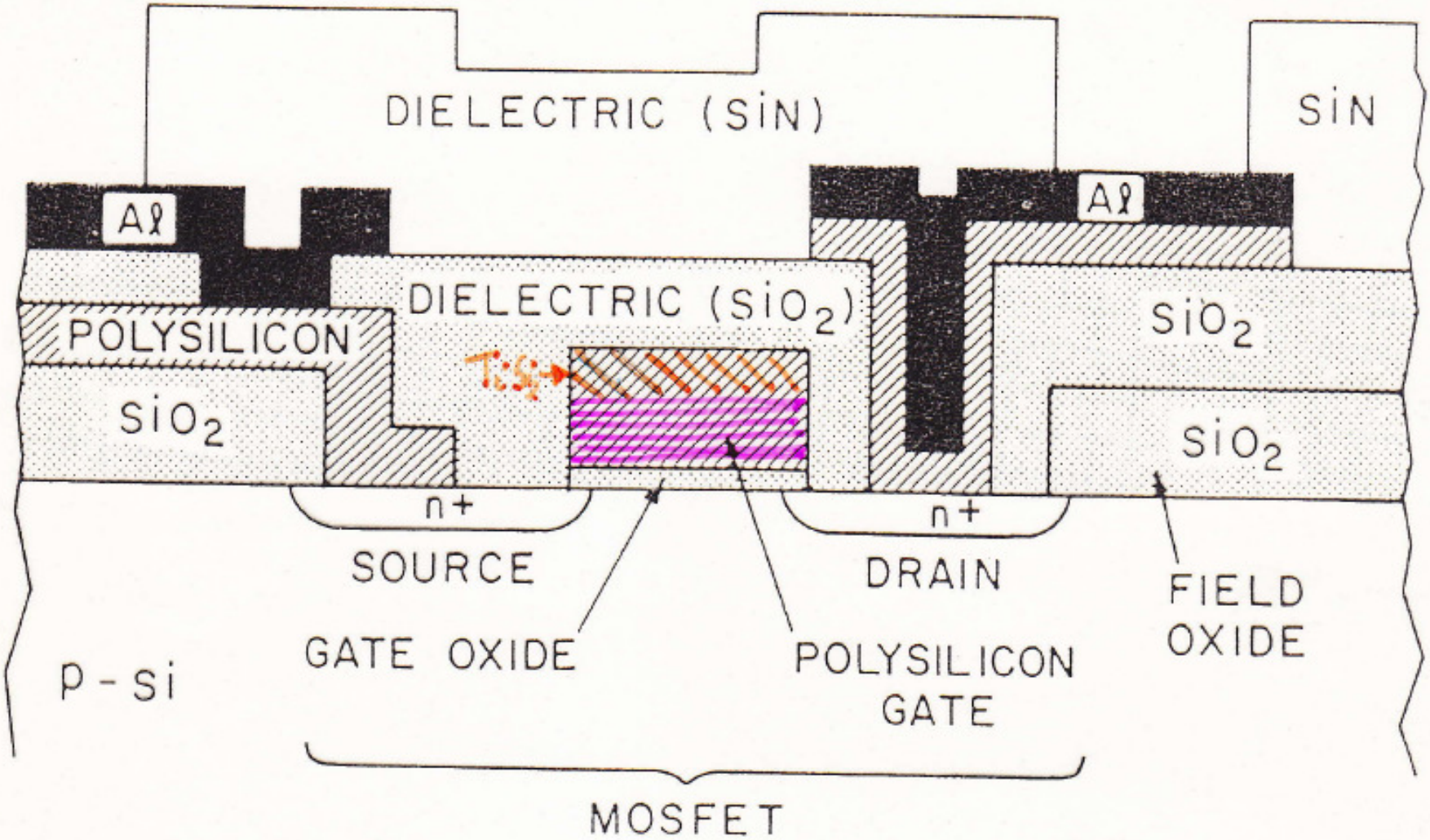
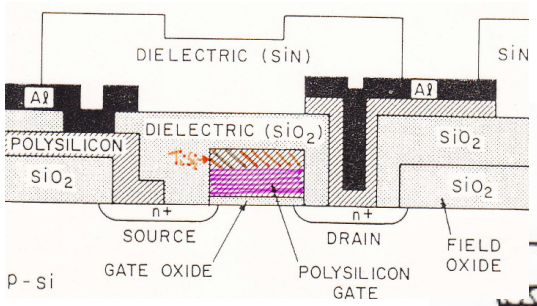
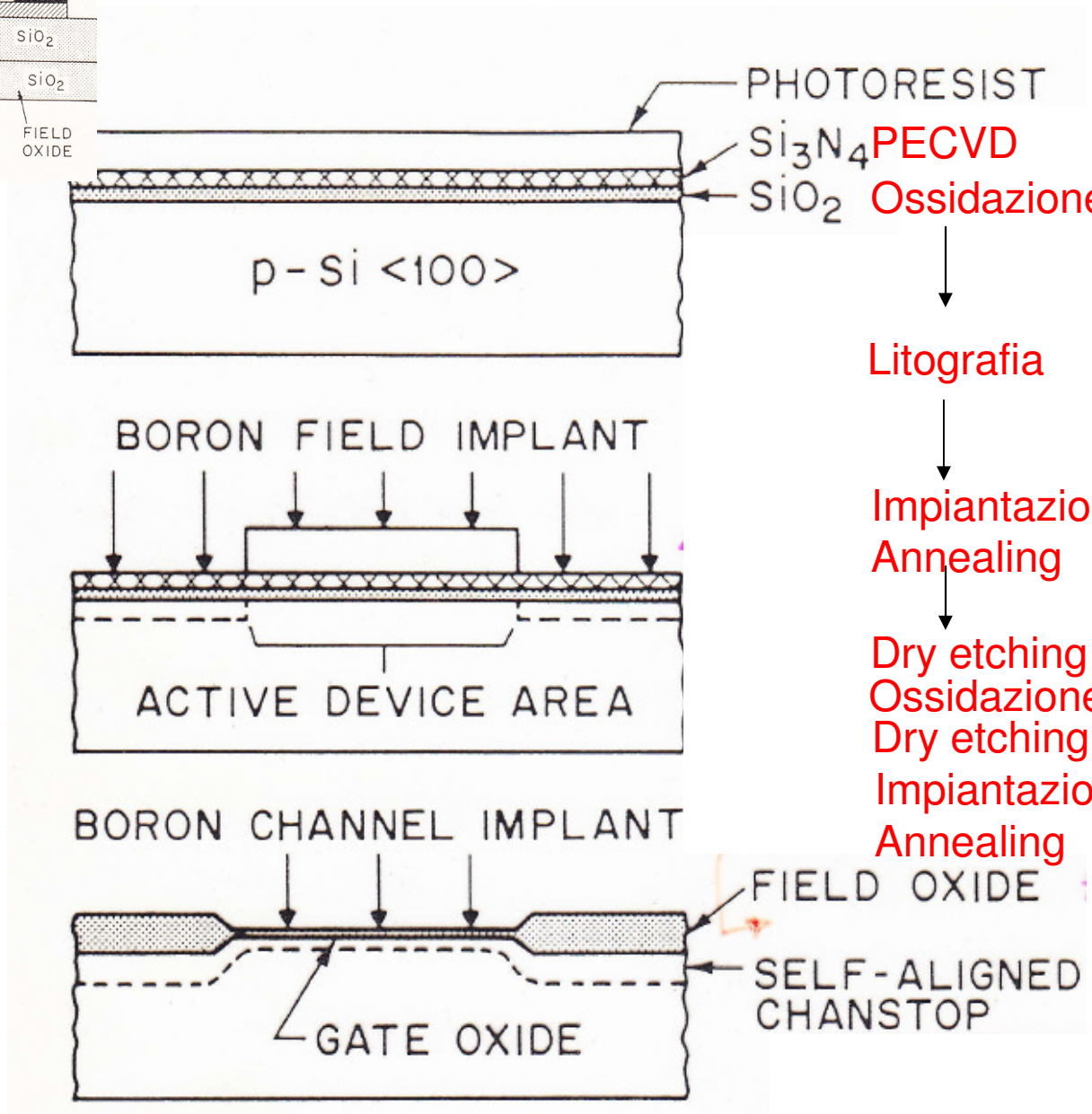


Fig. 1 Schematic view of a MOSFET cross section.





PECVD

Ossidazione termica

↓

Litografia

↓

Impiantazione p-type

Annealing

↓

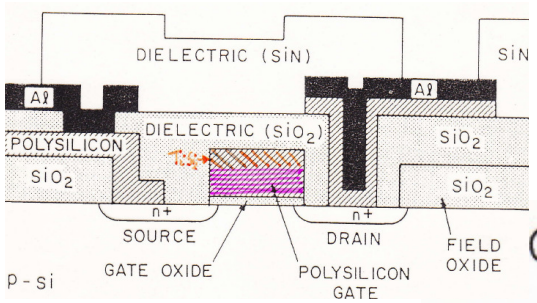
Dry etching

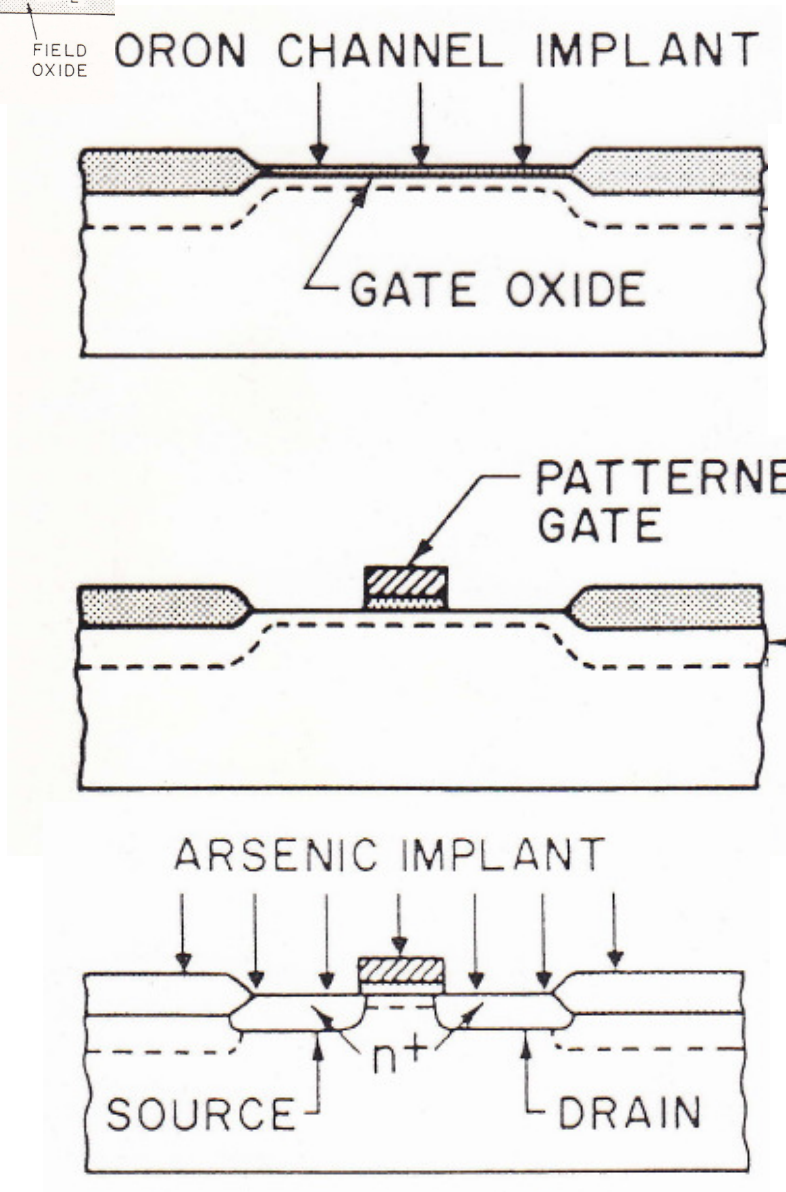
Ossidazione termica

Dry etching

Impiantazione p-type

Annealing





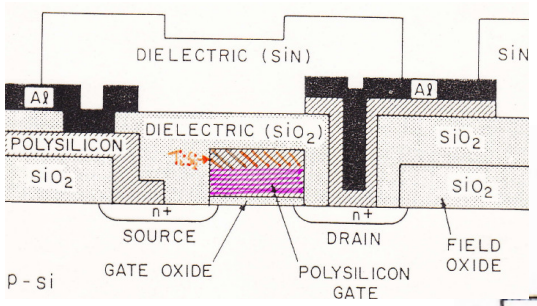
Litografia

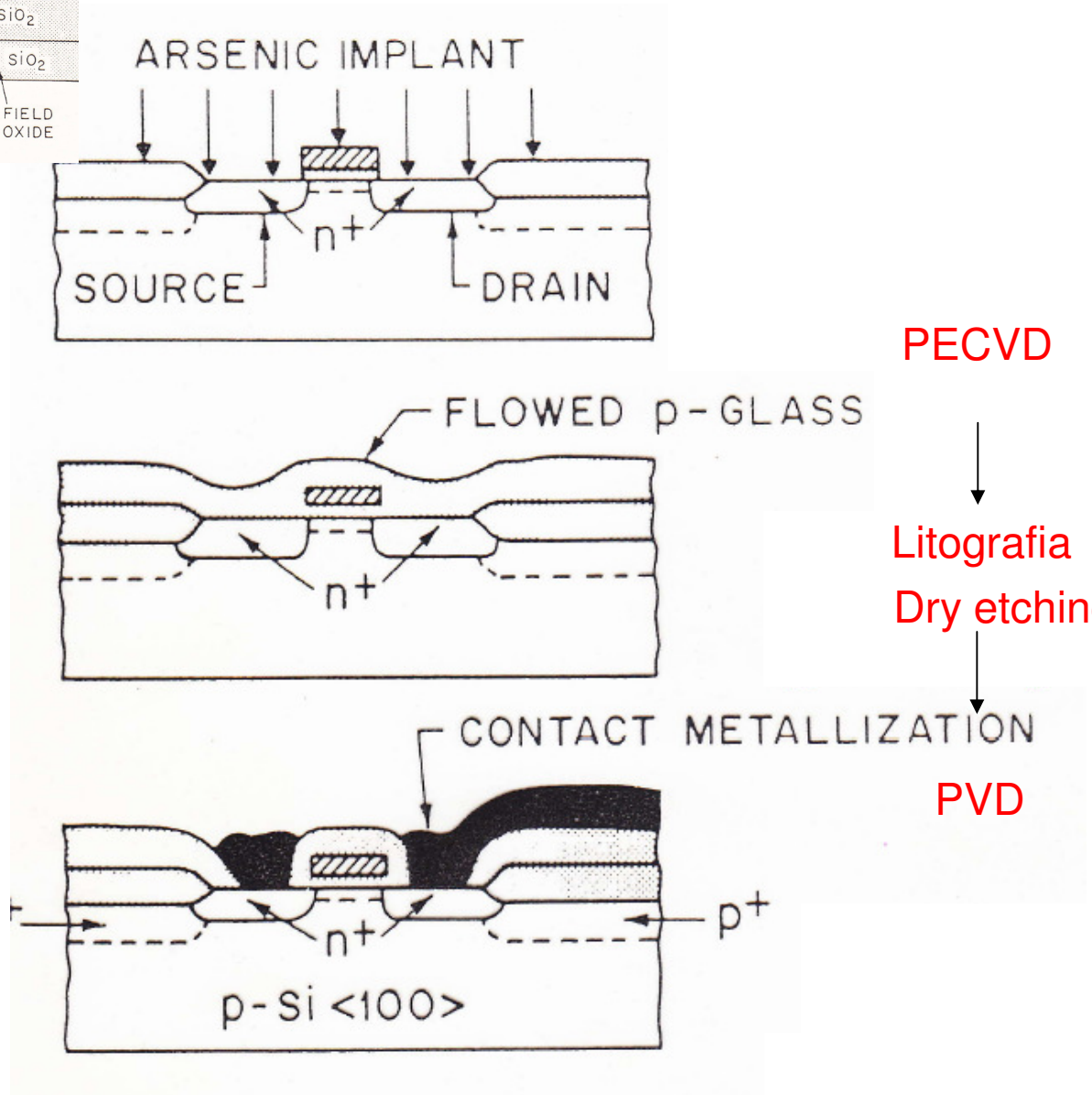
↓

PECVD
Dry etching

↓

Impiantazione n-type
Annealing





PECVD

↓

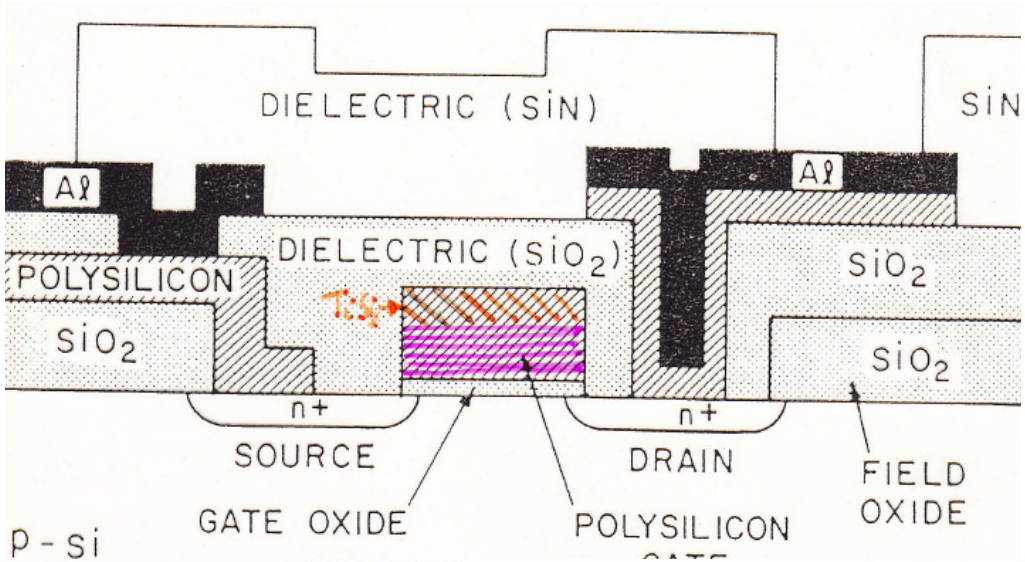
Litografia

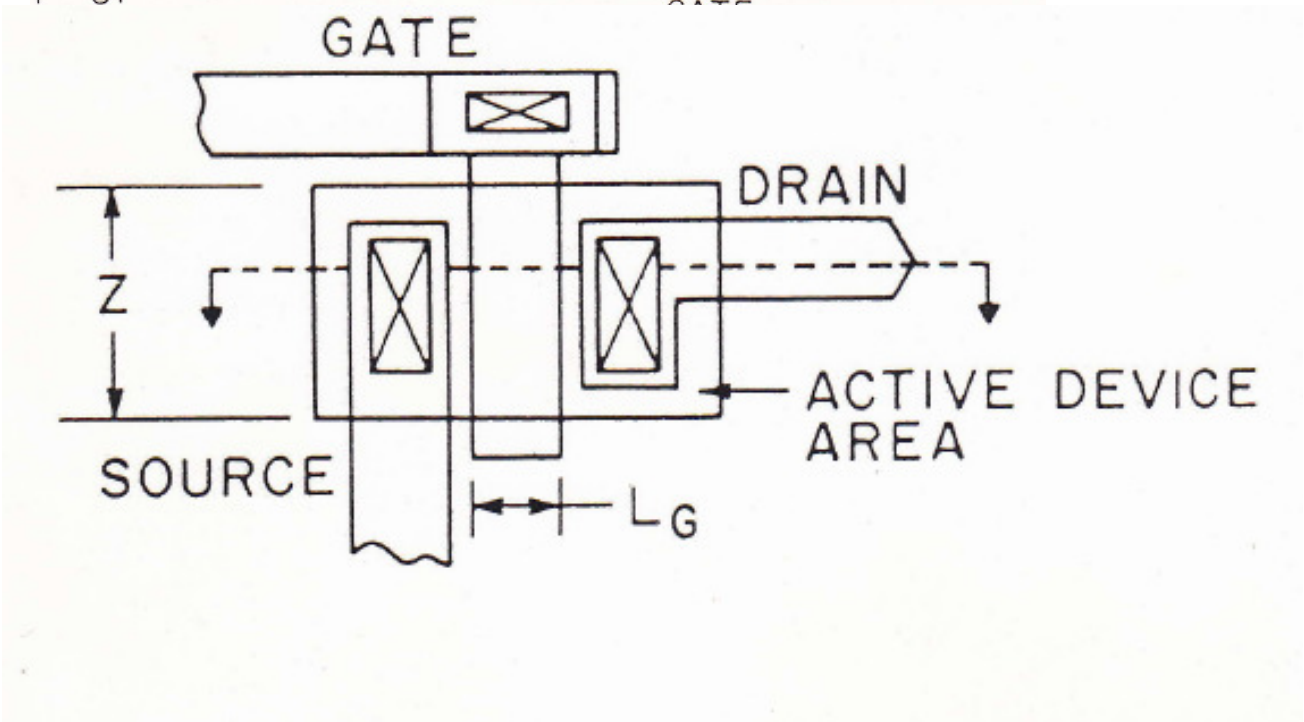
Dry etching

↓

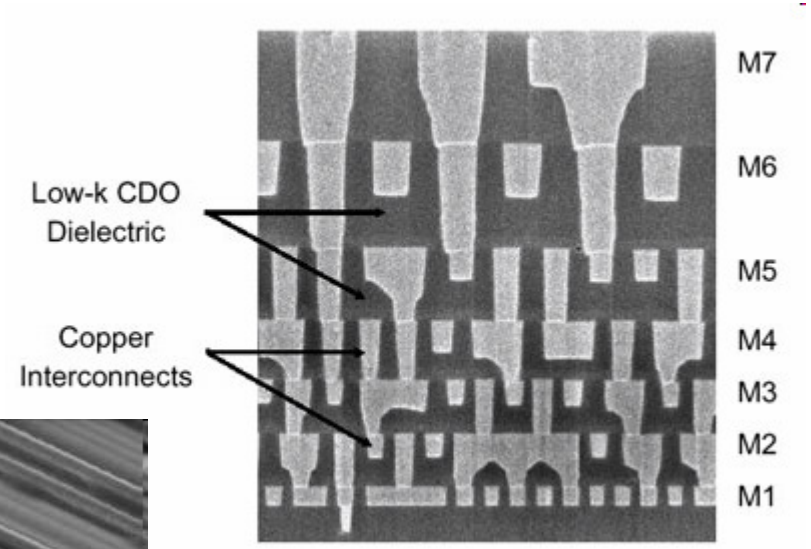
PVD

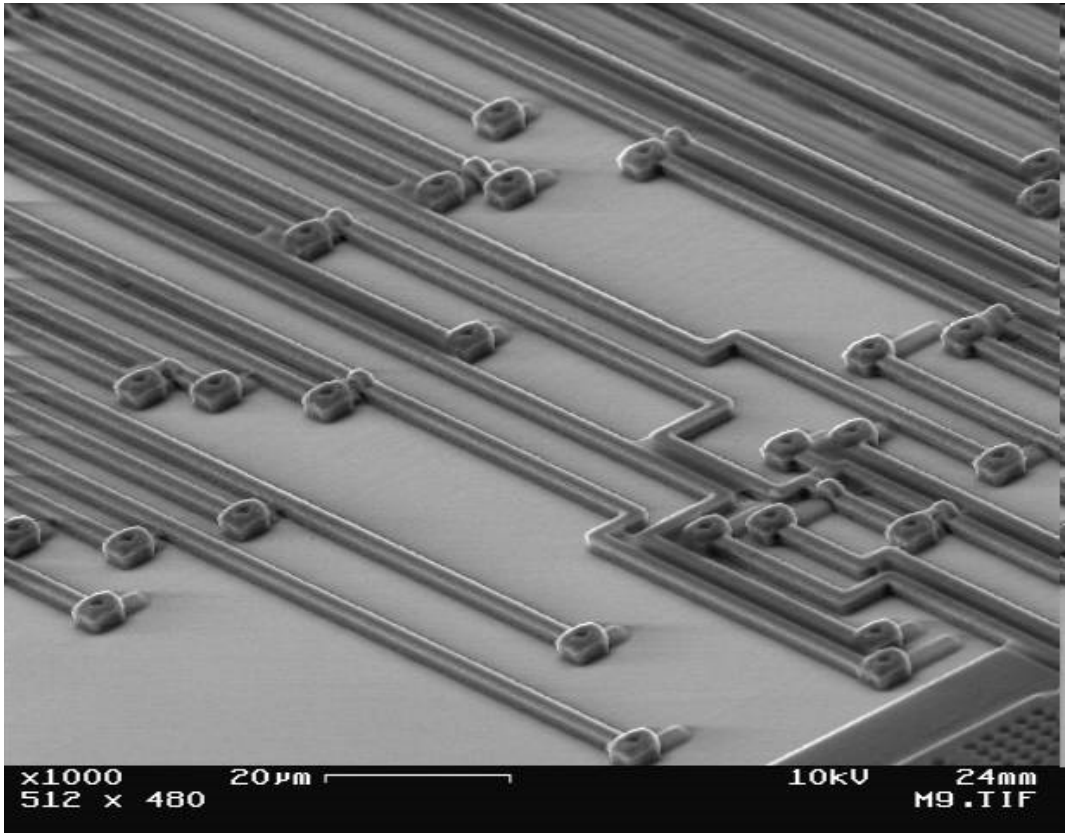
Metallizzazione



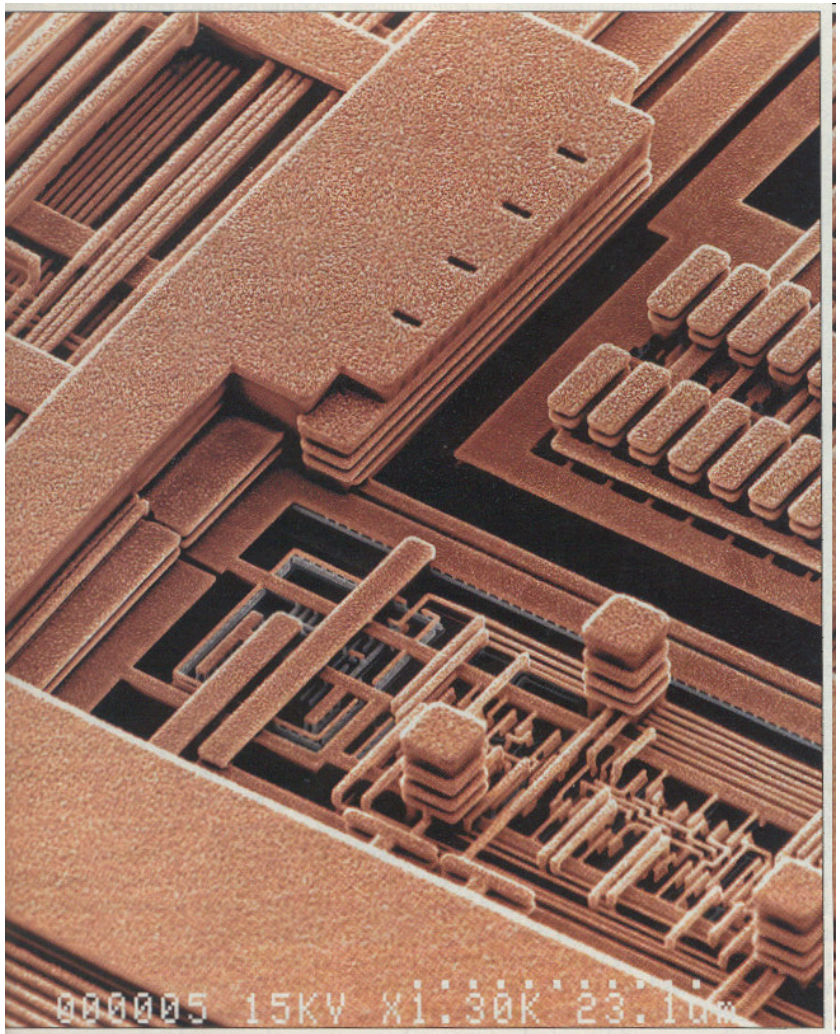
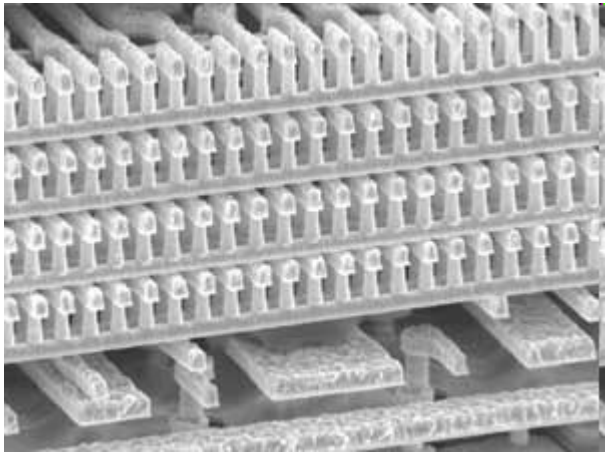


Metallizzazioni





Metallizzazioni



1] IBM Corp.'s new CMOS 7S process for manufacturing ICs uses copper for its six levels of nterconnections, and has effective transistor channel-lengths of only 0.12 µm. It is the first commercial fabrication process to use copper wires [see "The Damascus connection," p. 25].