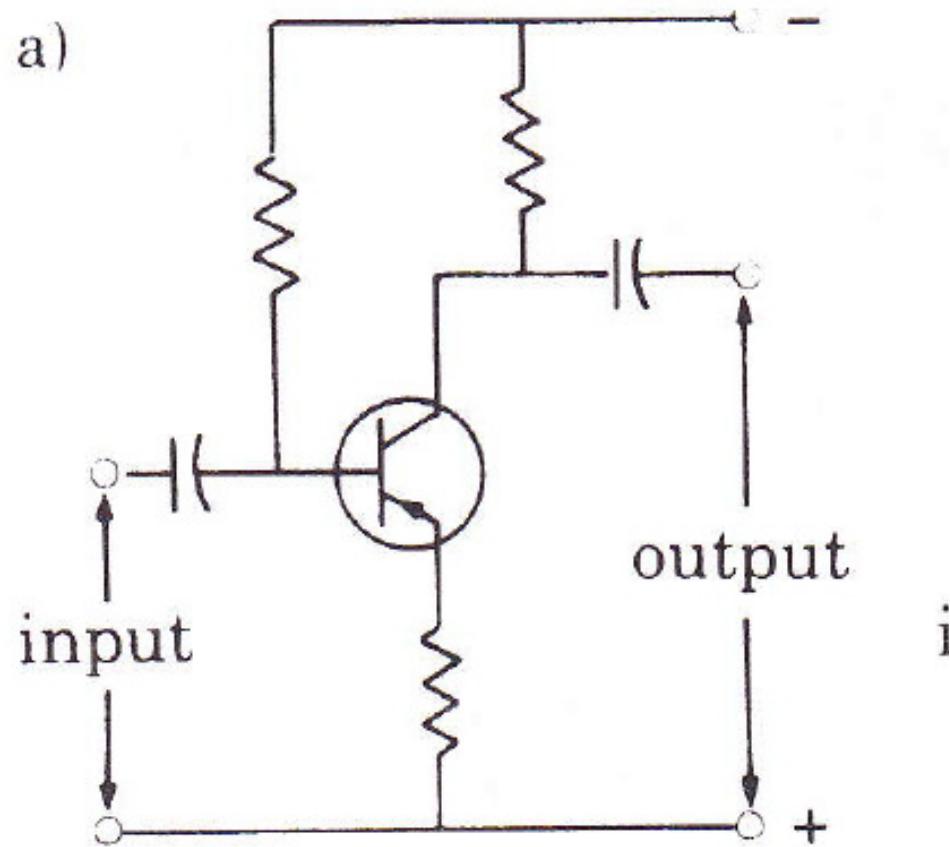
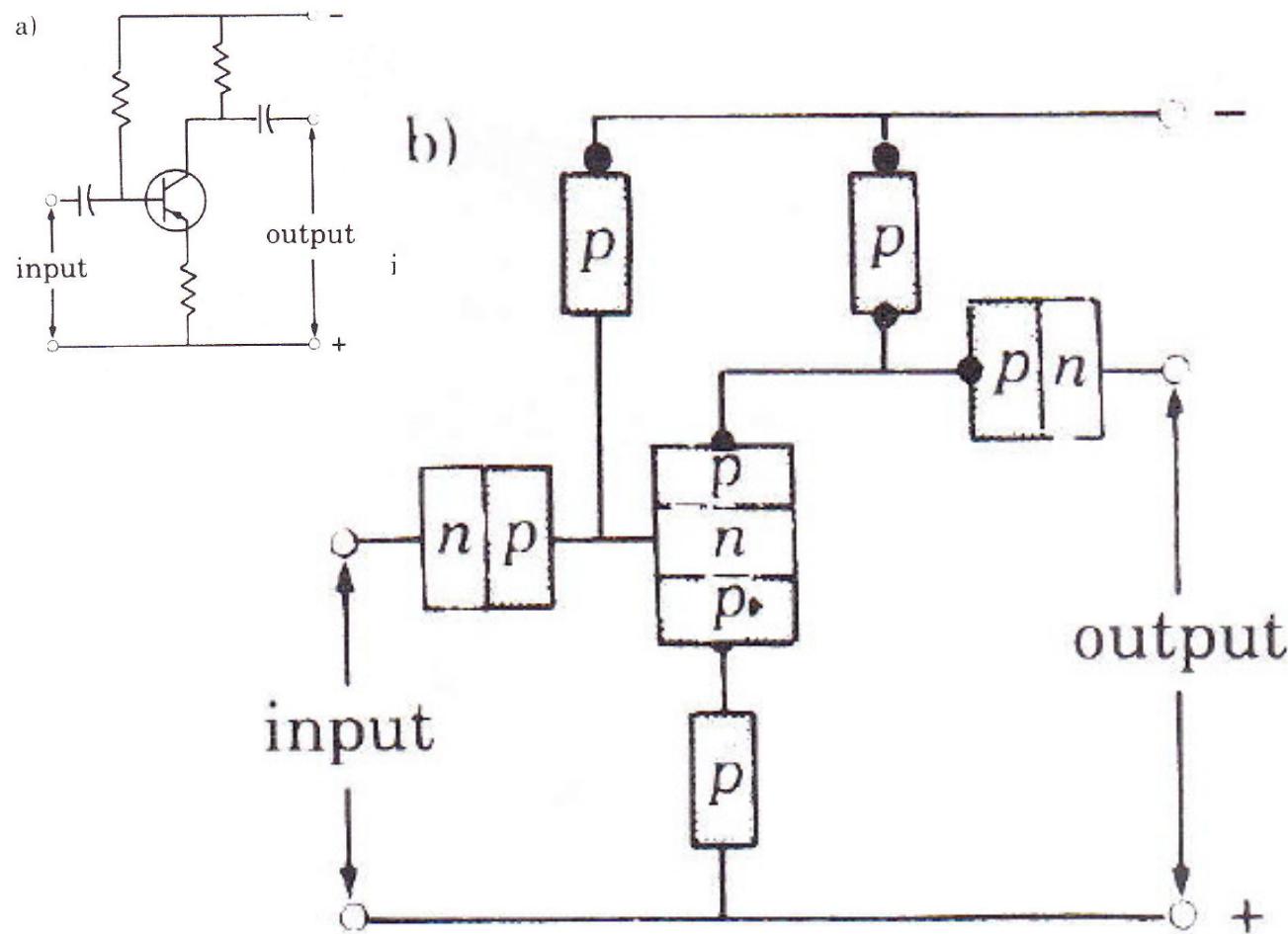


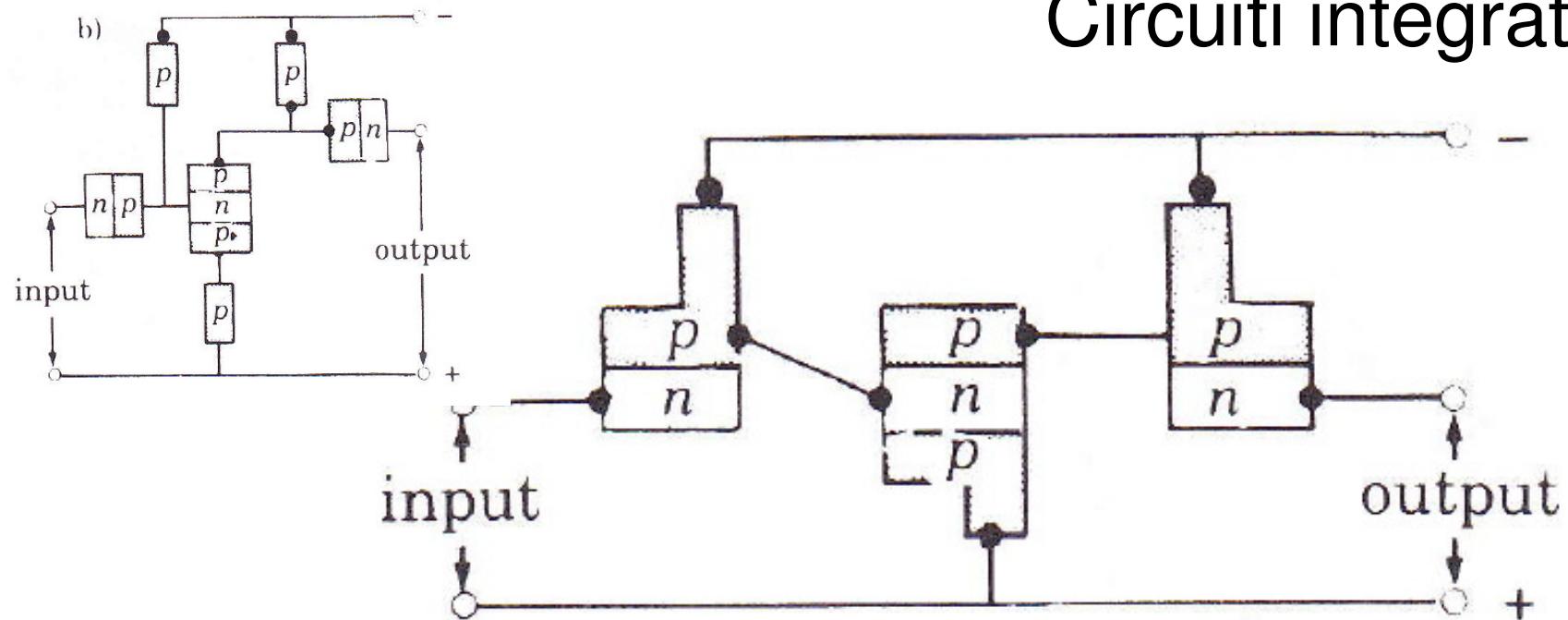
Circuiti integrati



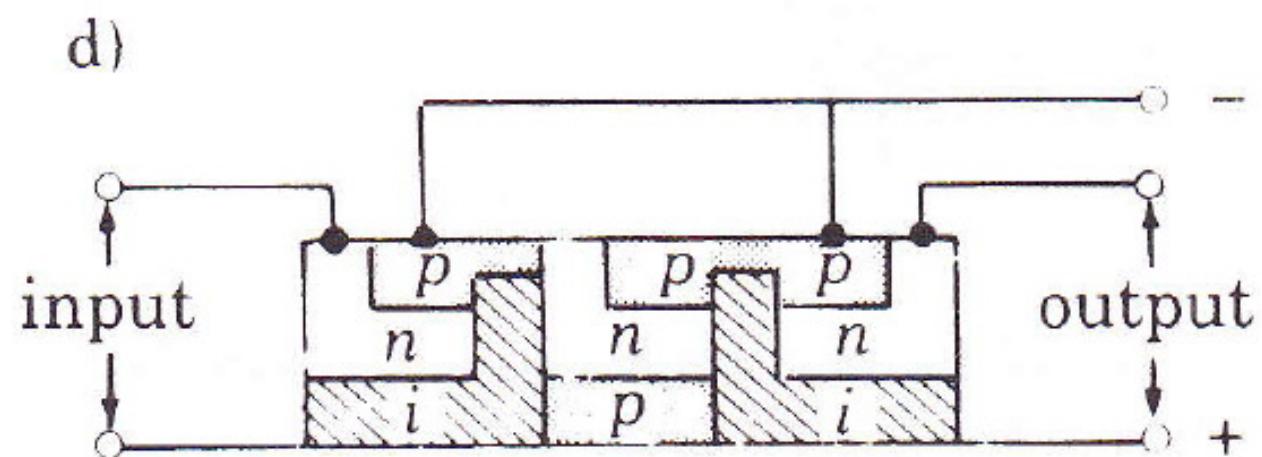
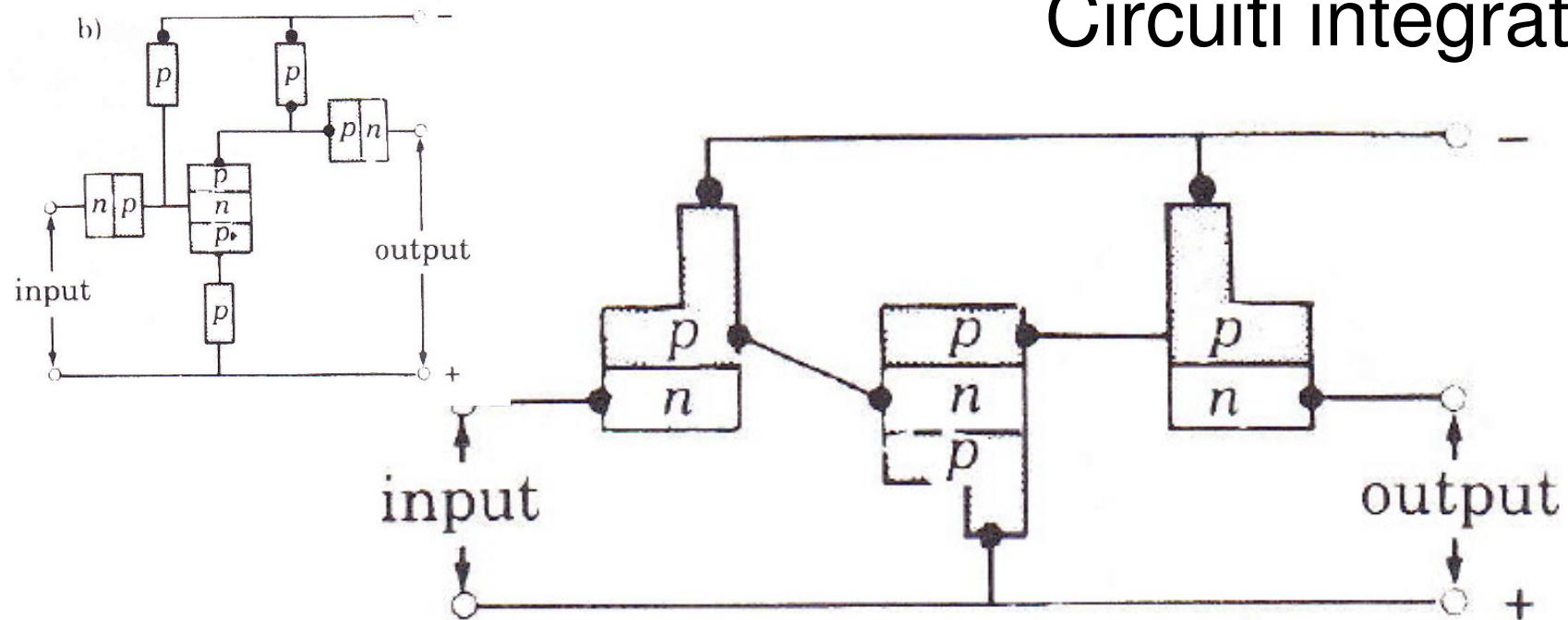
Circuiti integrati

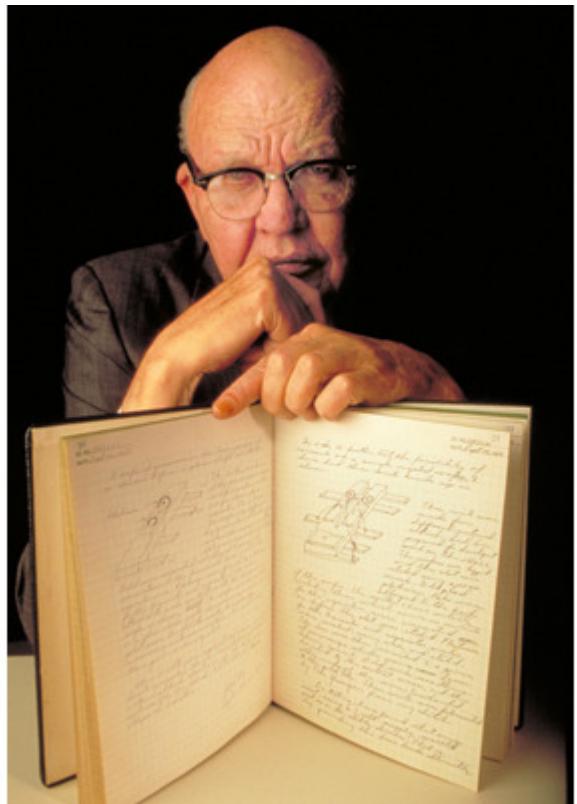


Circuiti integrati

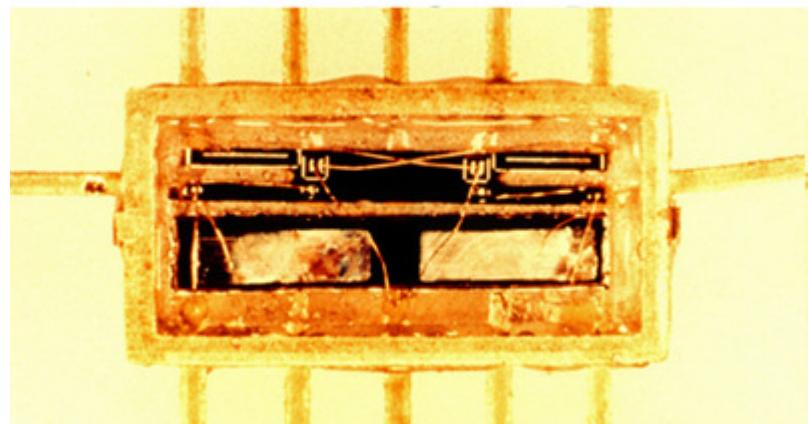
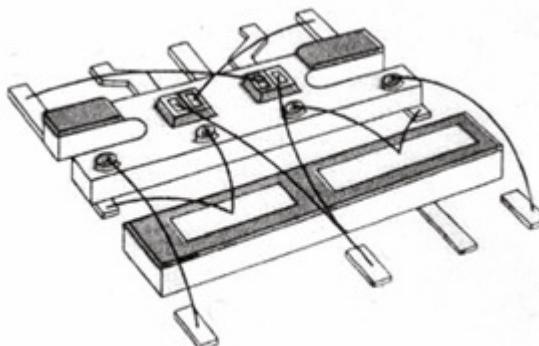


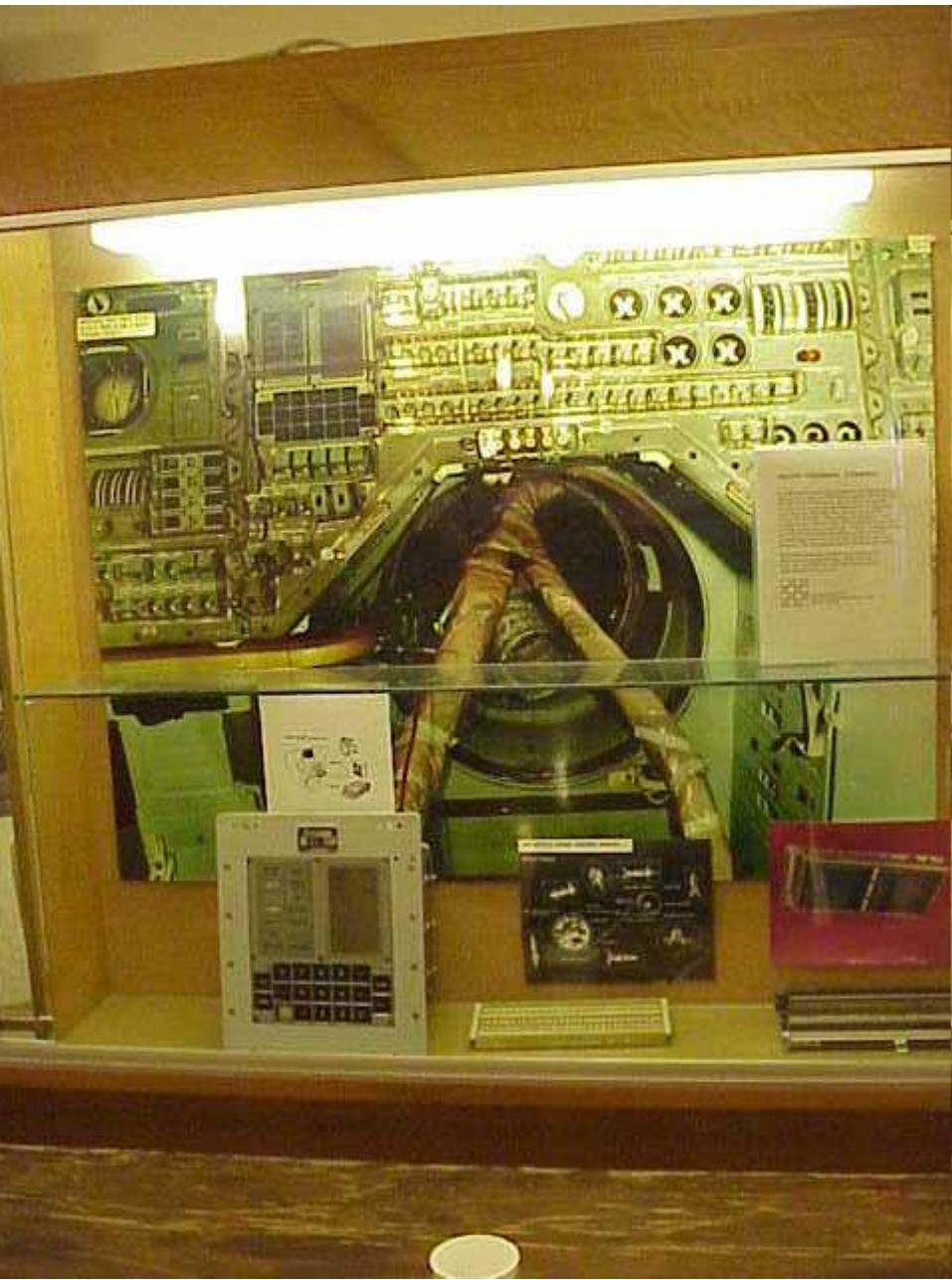
Circuiti integrati





Jack Kilby with his lab notebook open
at his first solid circuit drawing

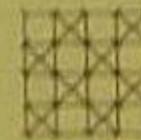




Apollo Guidance Computer

In 1960, NASA aircraft designers were given one cubic foot in which to build the computer which would land the ship onto the moon. (At the time, integrated circuits were a year old and transistorized computers were still new.) By 1962, they decided to go with integrated circuits — then costing \$1,000 each — but coming down to \$25 in 1965. The computer stored data in 15-bit words plus a parity bit. It had a memory cycle time of 11.7 microseconds, utilizing 2,000 words of erasable core memory and 36,000 words of read-only memory. The magnesium frame is hermetically sealed.

The DSKY computer interface was used by the astronauts for programming. They used the verb and noun buttons with two digit codes to create desired instructions.



From the collection of
The Computer Museum History Center
X37-81-3186.R3

First IC Computer
2 Kbytes RAM
36 Kbytes ROM

Circuiti integrati

Small-Scale Integration (SSI), <100 transistors 1960-1965

Medium-Scale Integration (MSI). 100-3000 transistors 1965-1975

Large-Scale Integration (LSI) 3000-100000 transistors 1975- 1980

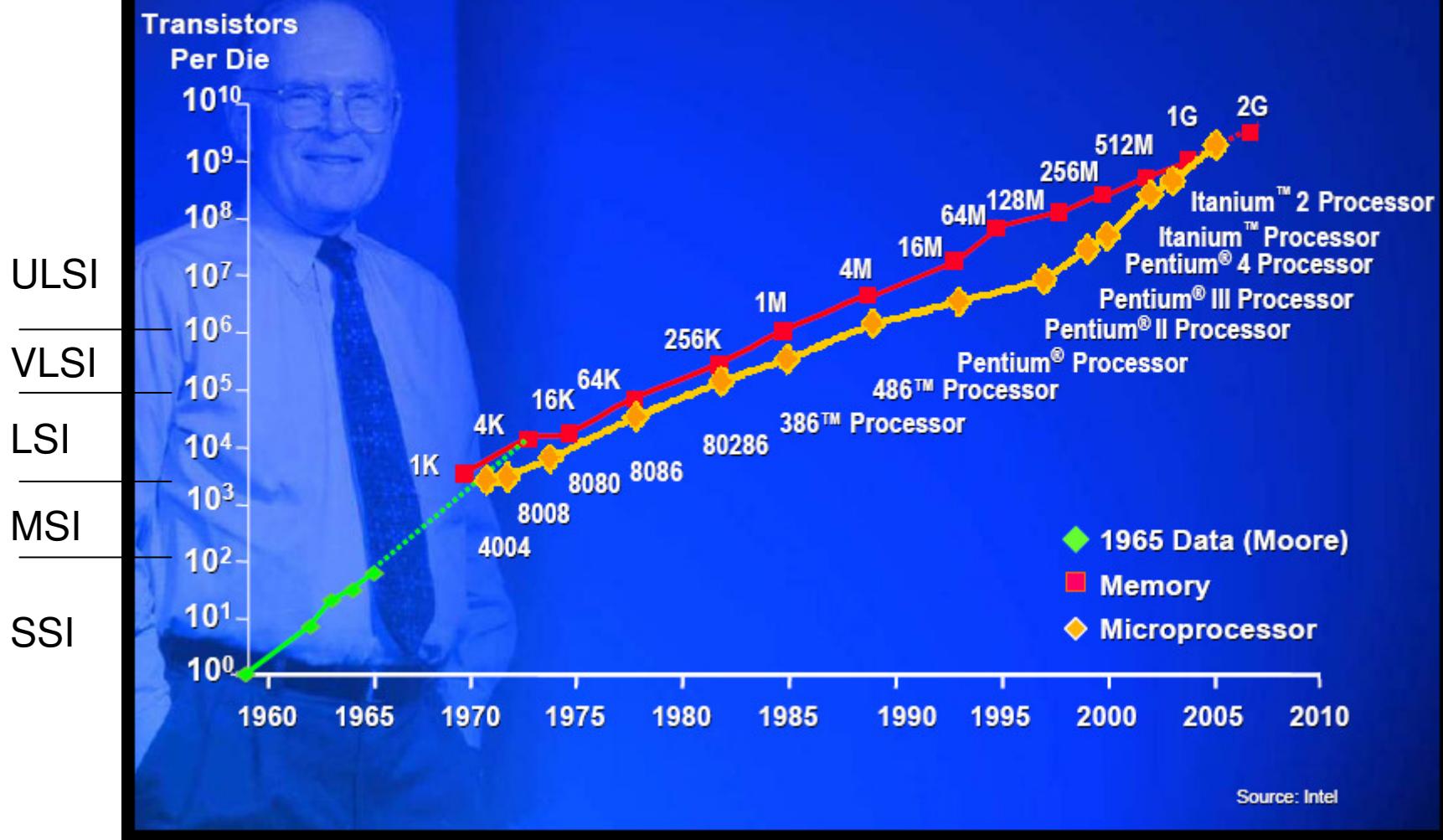
Very -LSI (VLSI) 100000-1000000 1980-2000

Ultra -LSI (ULSI) more than 1 million transistors.

Wafer Scale Integration (WSI) entire silicon wafer for a single "super-chip".

Three Dimensional IC (3D-IC) has two or more layers of active electronic components that are integrated both vertically and horizontally into a single circuit.

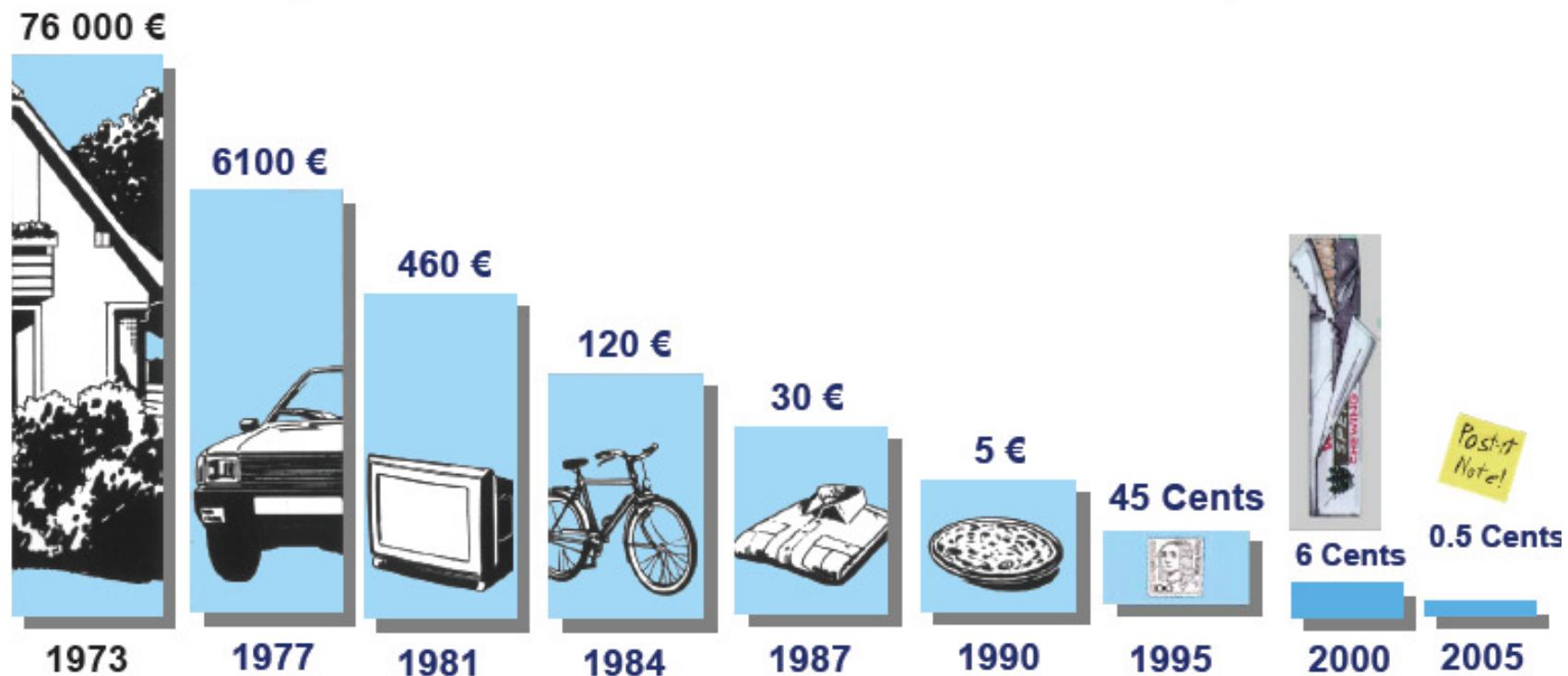
Moore's Law - 2005

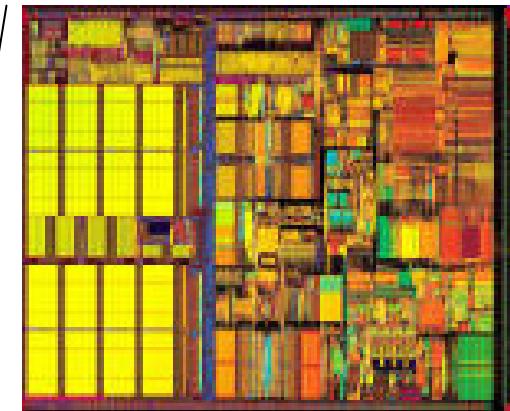
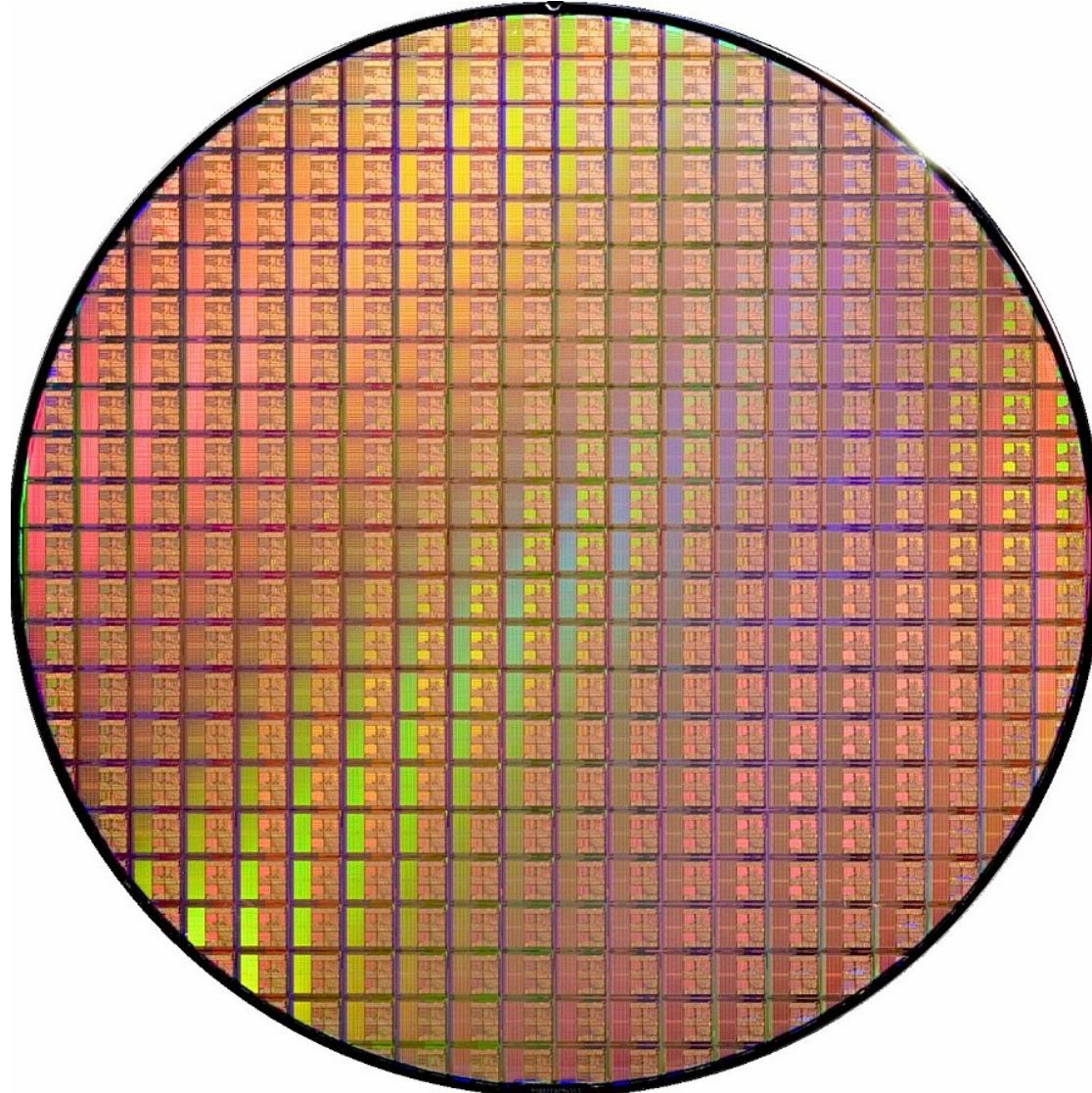


The microelectronics success story

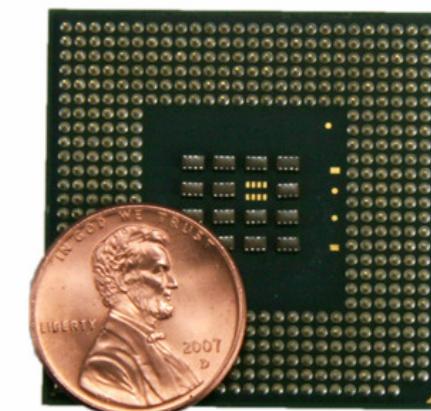
A cost reduction unique in the industry history

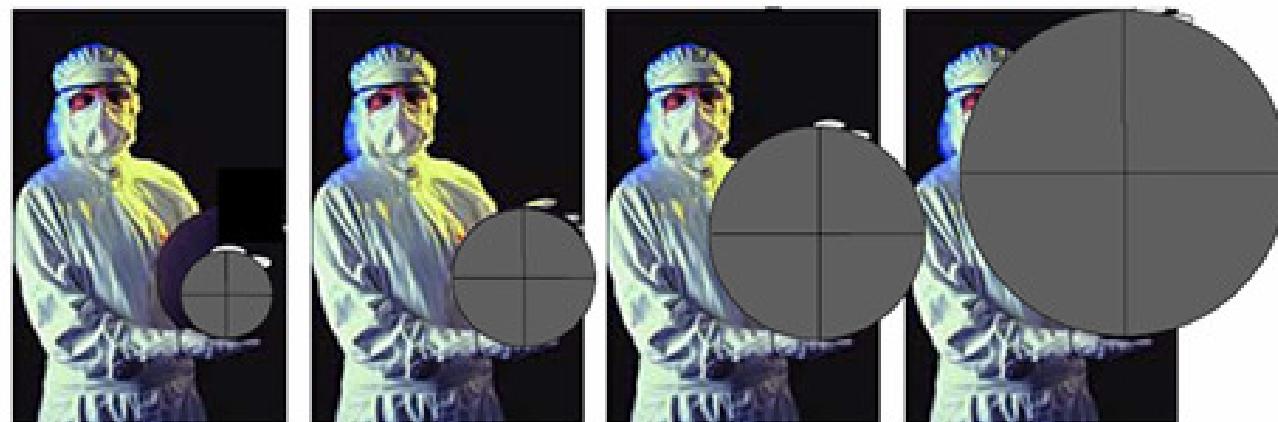
PRIZE EVOLUTION OF 1 Million transistors





Pentium 3
9.5 MTransistors





200mm/1990

--- (125/150mm - 1981)

9 yrs + 2 yrs delay*

300mm/2001

11 yrs + 0 yrs delay

450mm/2012

9 yrs + 0 yrs delay

675mm/2019?

→

Costruzione di 1 MOSFET

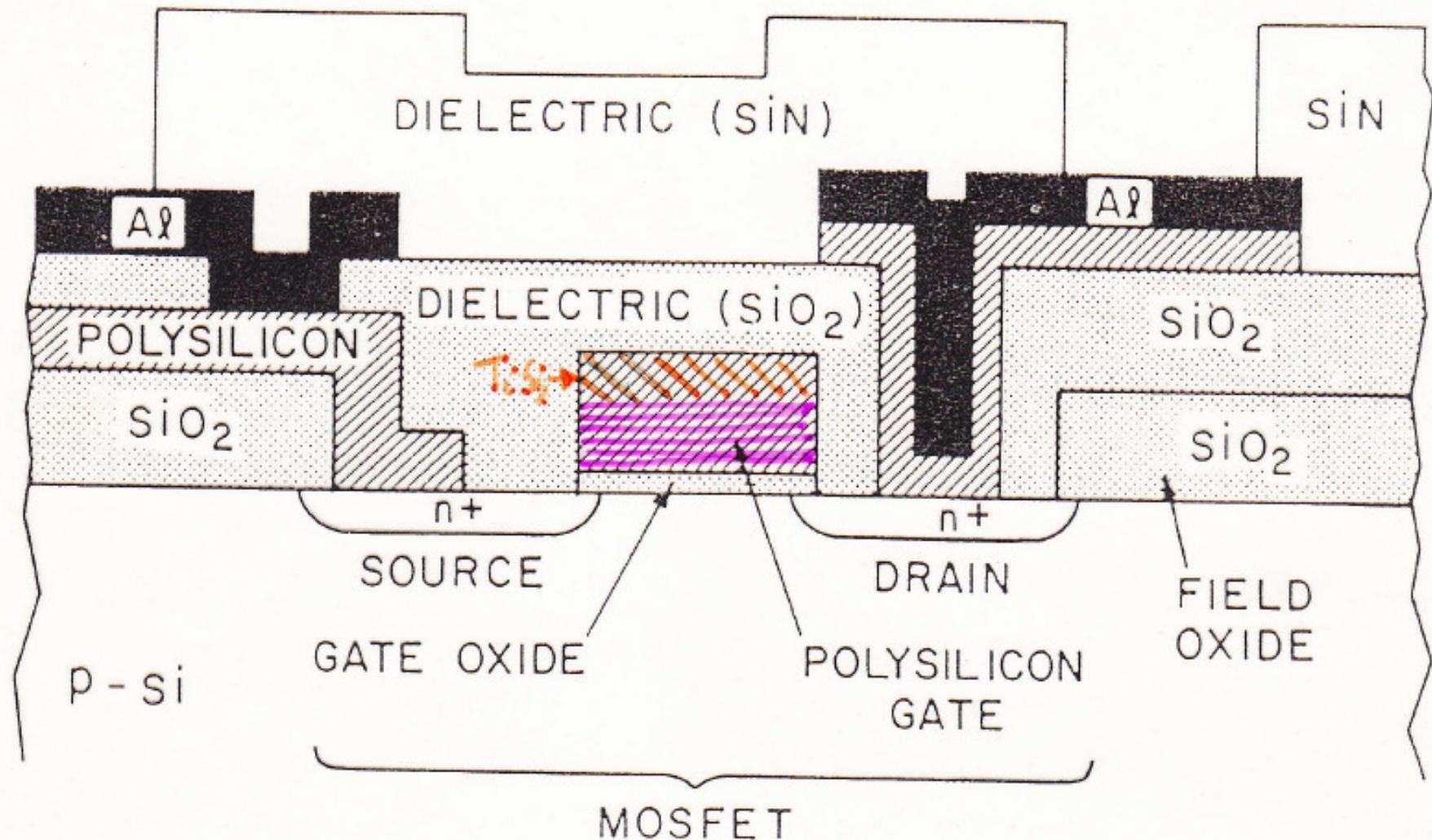


Fig. 1 Schematic view of a MOSFET cross section.

Crescita ossido termico (Gate oxide)

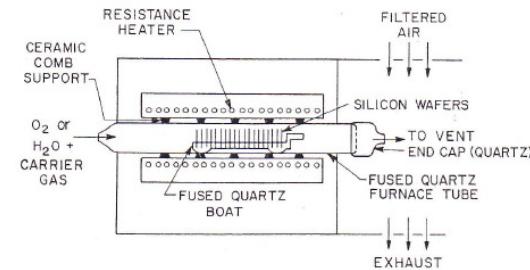
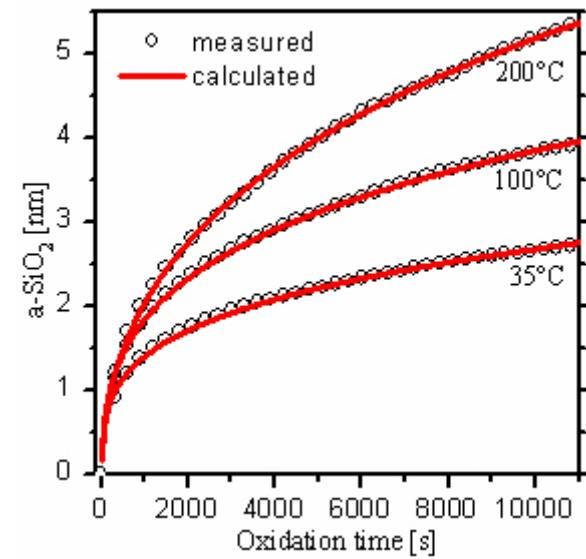
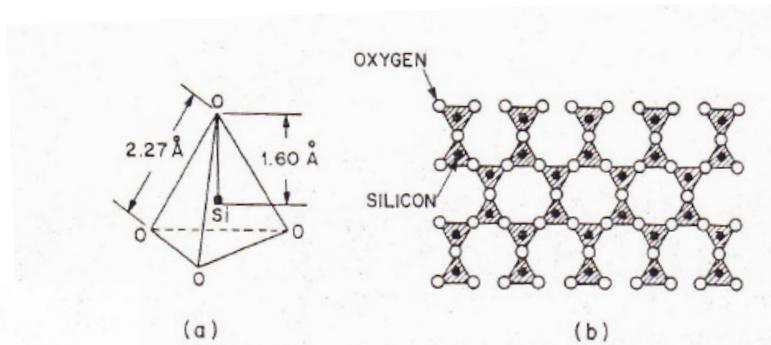


Fig. 2 Schematic cross section of a resistance-heated oxidation furnace. The silicon wafer loading area is shown in a laminar hood.³





Problem

If a silicon oxide layer of thickness x is grown from thermal oxidation, what is the thickness of silicon being consumed?

Solution

The volume of 1 mole silicon is

$$\frac{\text{Molecular weight of Si}}{\text{Density of Si}} = \frac{28.09 \text{ g/mole}}{2.33 \text{ g/cm}^3} = 12.06 \text{ cm}^3/\text{mole}.$$

The volume of 1 mole silicon dioxide is

$$\frac{\text{Molecular weight of } \text{SiO}_2}{\text{Density of } \text{SiO}_2} = \frac{60.08 \text{ g/mole}}{2.21 \text{ g/cm}^3} = 27.18 \text{ cm}^3/\text{mole}.$$

Since 1 mole silicon is converted to 1 mole silicon dioxide,

$$\frac{\text{Thickness of Si} \times \text{area}}{\text{Thickness of } \text{SiO}_2 \times \text{area}} = \frac{\text{volume of 1 mole of Si}}{\text{volume of 1 mole of } \text{SiO}_2}$$

$$\frac{\text{Thickness of Si}}{\text{Thickness of } \text{SiO}_2} = \frac{12.06}{27.18} = 0.44$$

Thickness of silicon = 0.44(thickness of SiO_2).

That is, to grow 1000 Å of silicon dioxide, a layer of 440 Å of silicon is consumed.

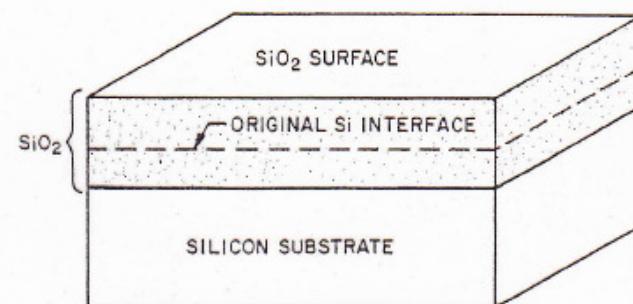
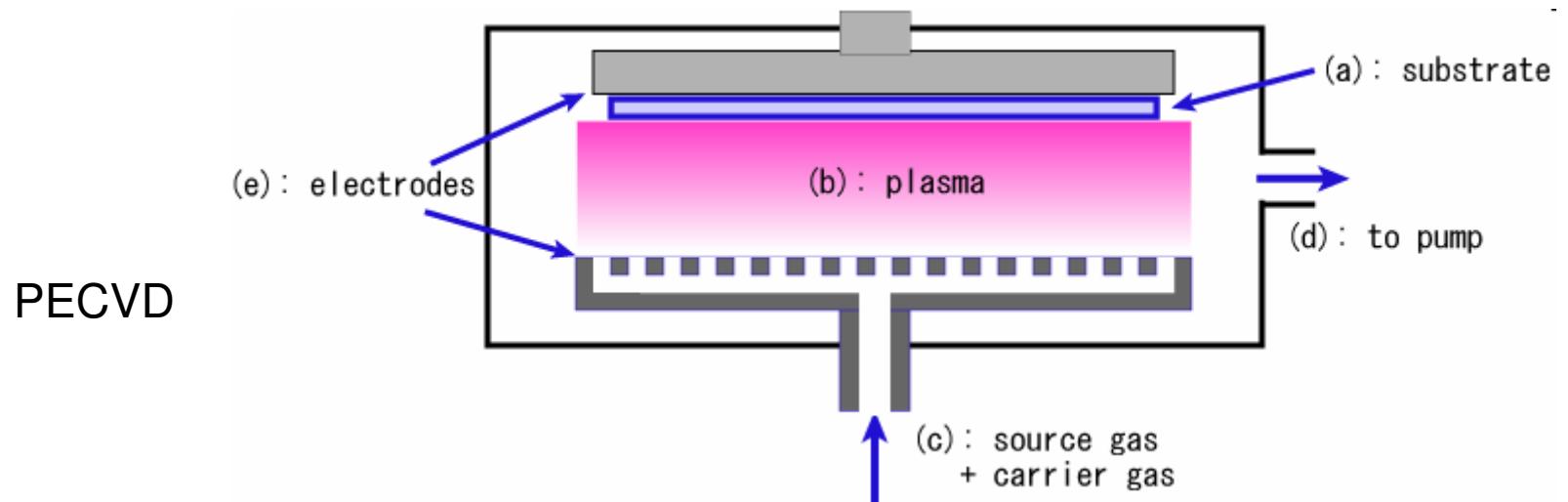
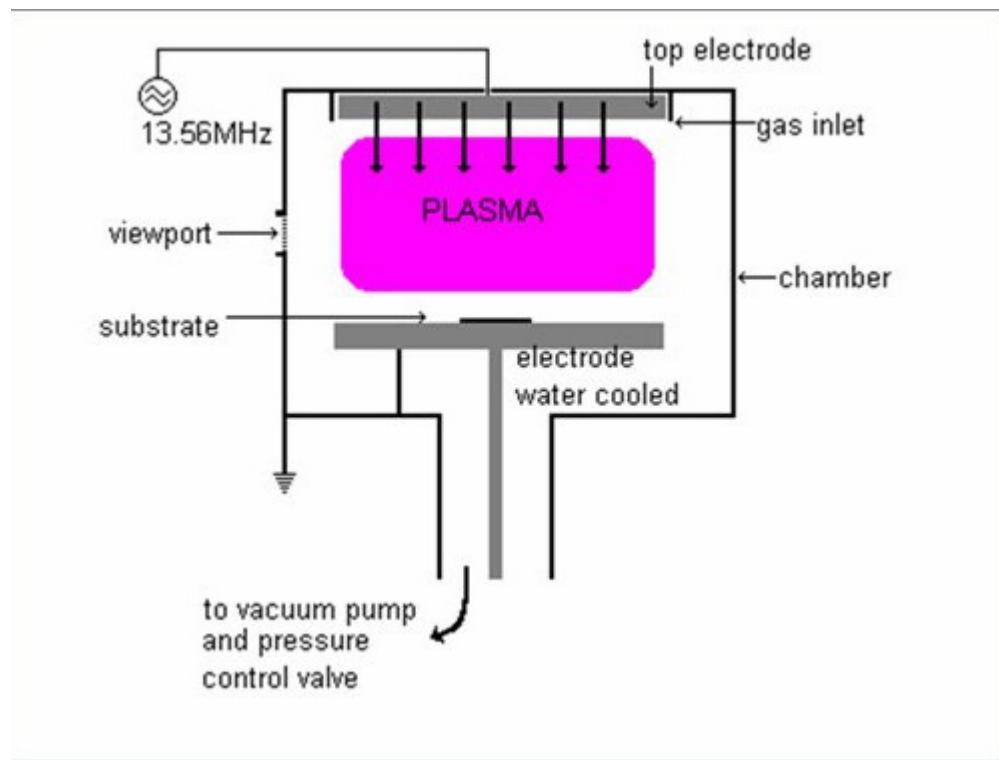
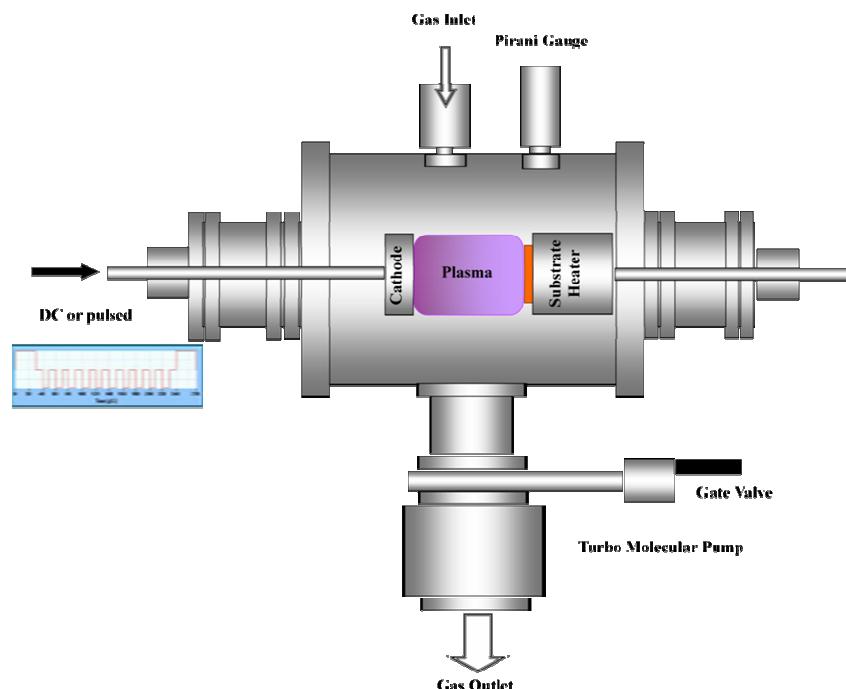


Fig. 3 Growth of silicon dioxide by thermal oxidation.²



Deposito di SiO₂, Si₃N₄, polysilicon

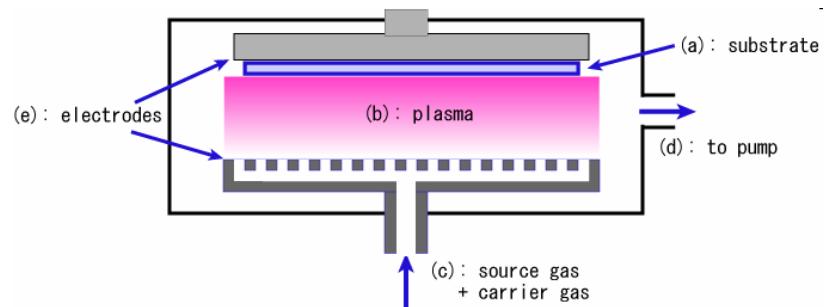
Plasma enhanced chemical vapor deposition (PECVD)



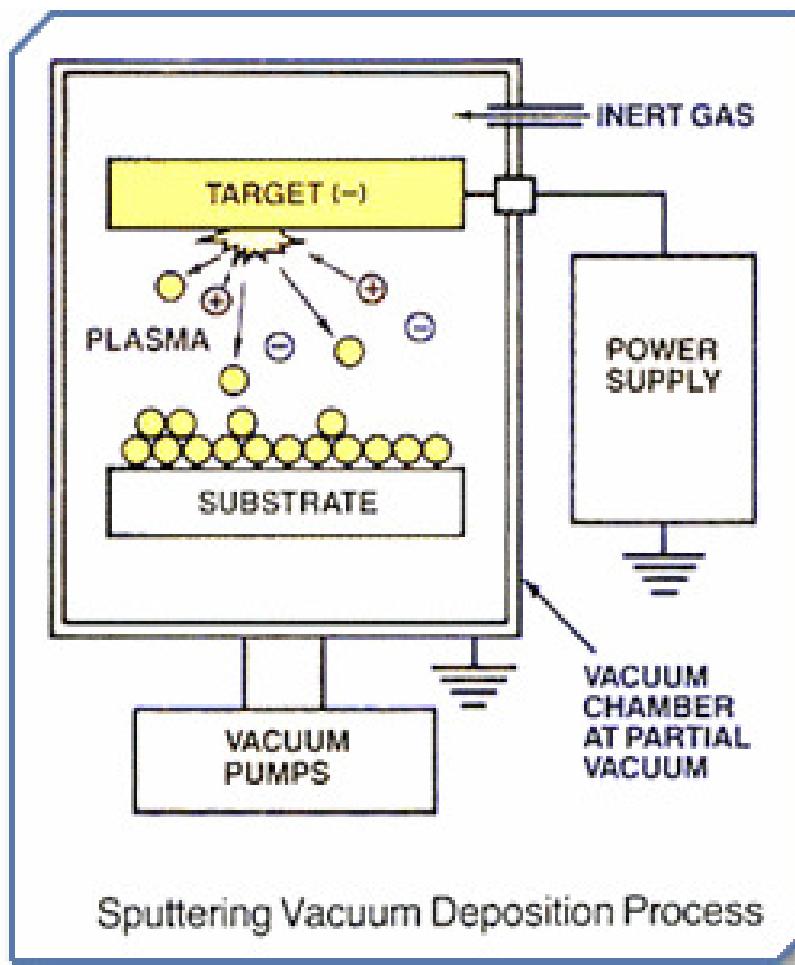
Schematic diagram of the pulsed-DC PECVD system

Vantaggi Plasma:

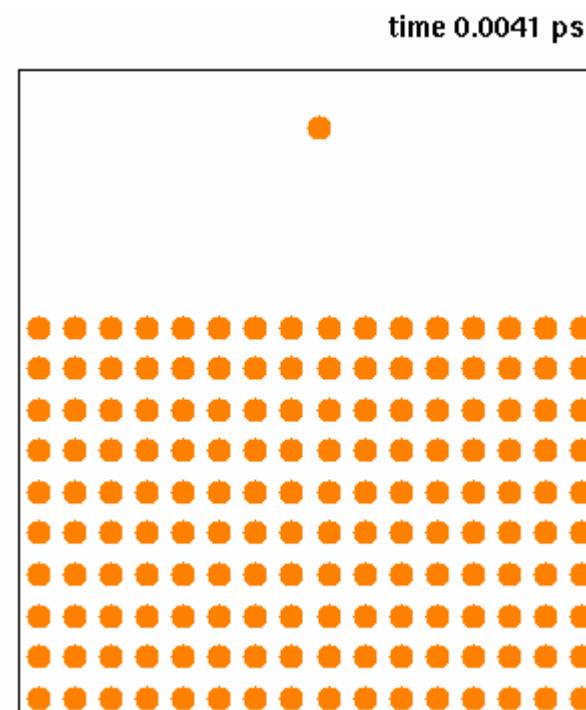
- 1) Formazione radicali
- 2) Bombardamento ionico che produce rimozione e planarizzazione.



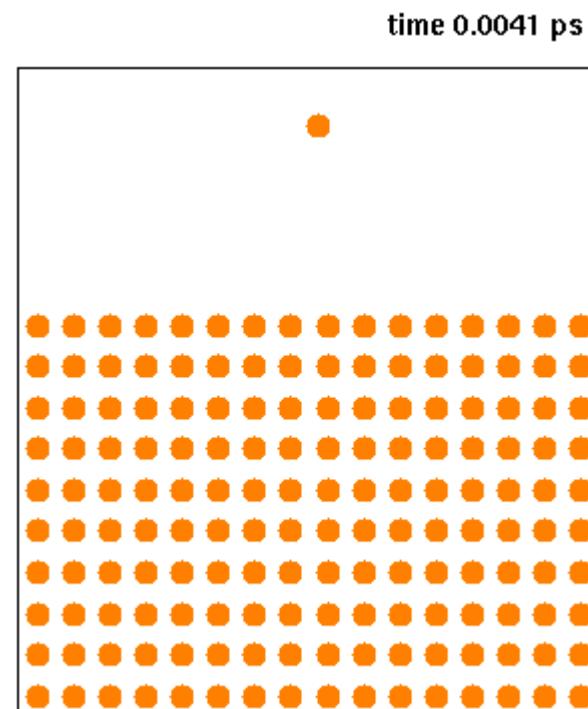
Deposito di metalli (sputtering) Physical Vapor Deposition (PVD)



Physical Vapor Deposition (PVD)

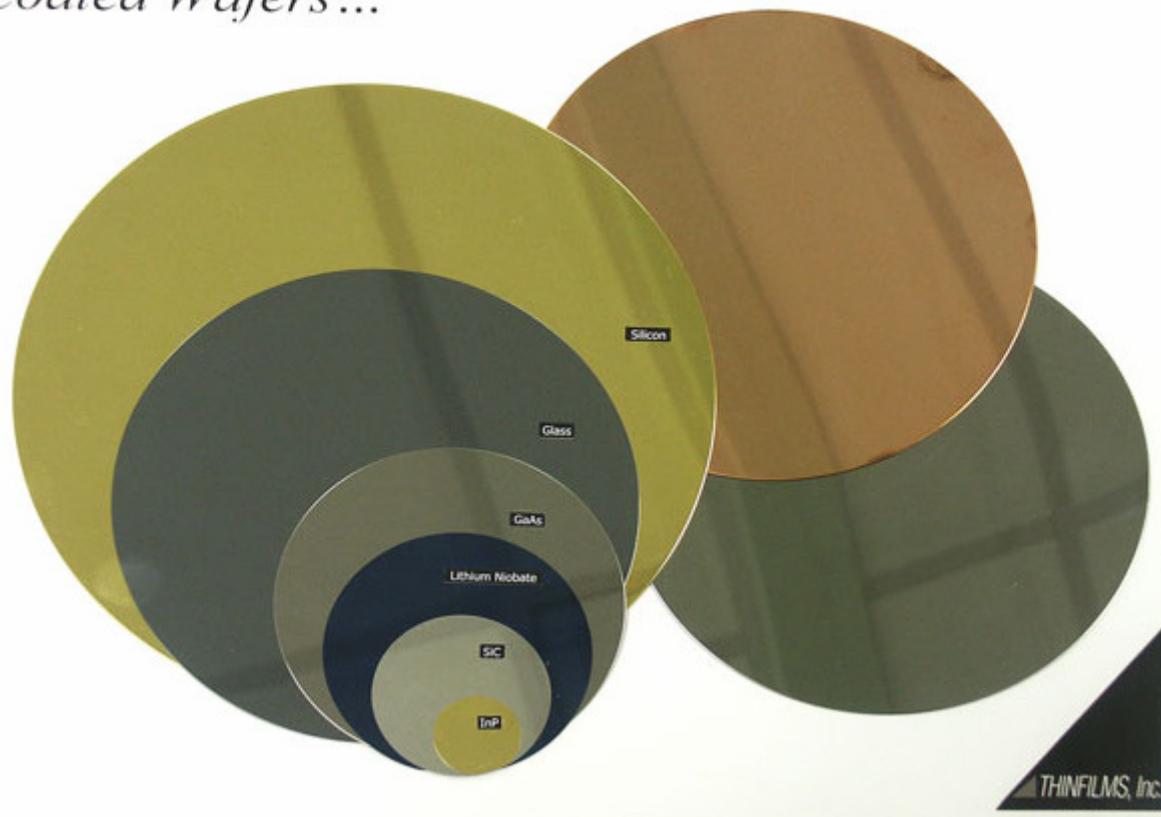


Physical Vapor Deposition (PVD)

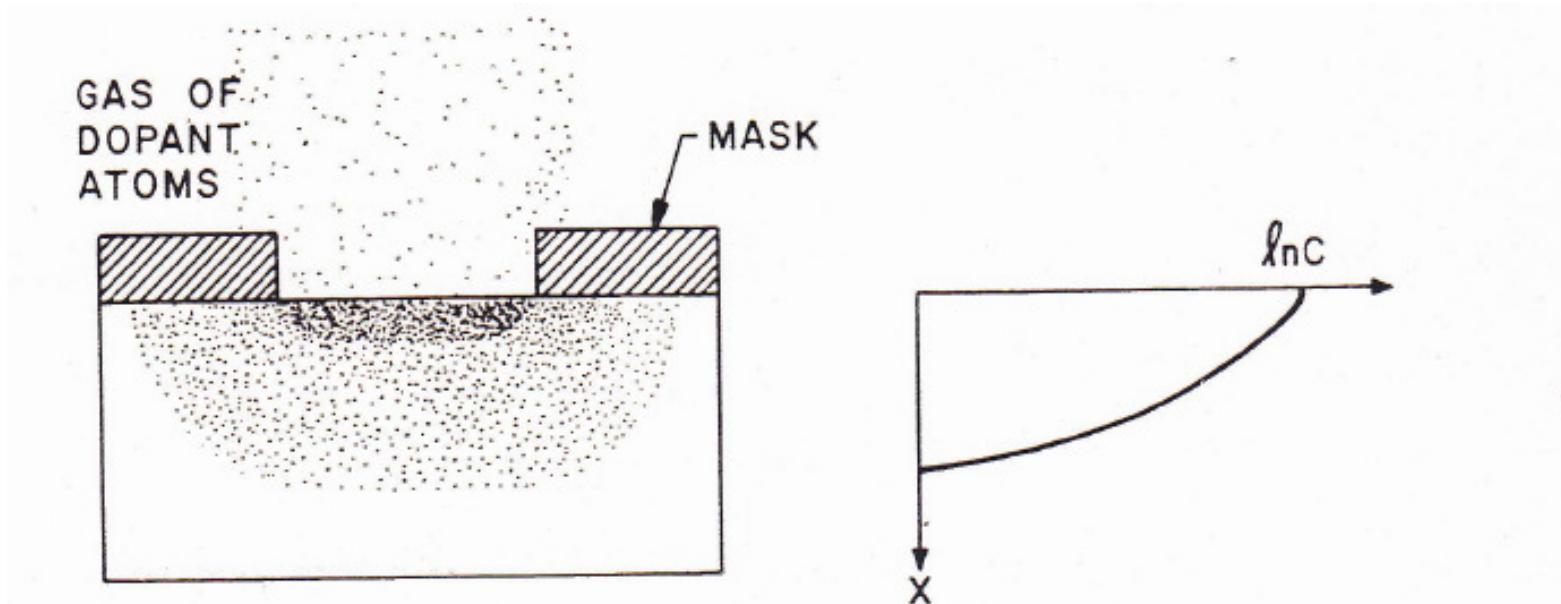


TiW-Ni-Au, Ti-NiV-Au, Ti-Pt-Au, Cr-Ni-Au and TiW-Ni-Ag

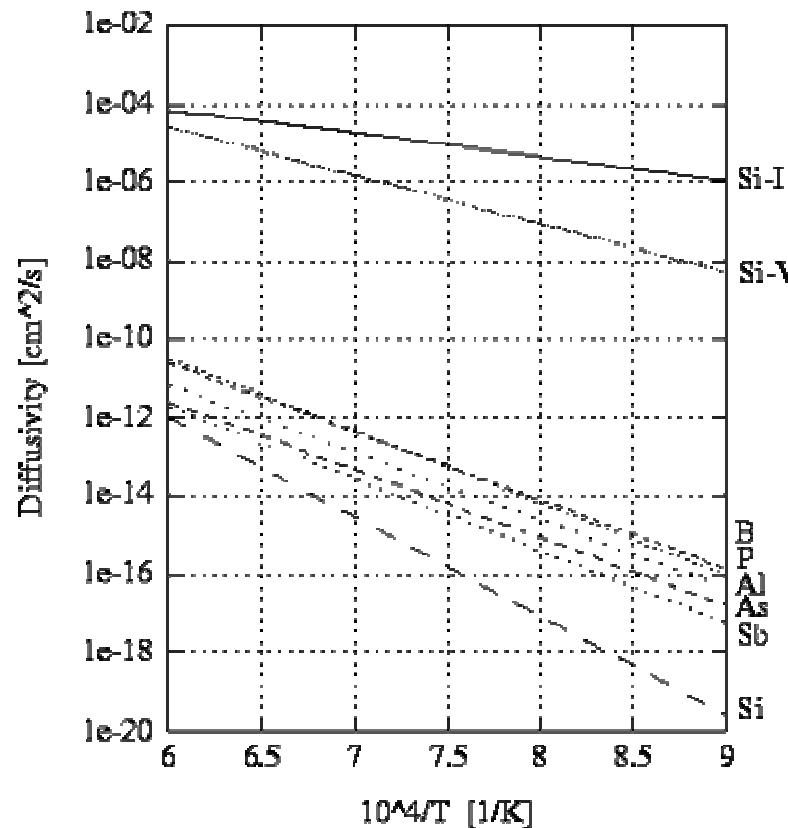
Coated Wafers...



Drogaggio per diffusione



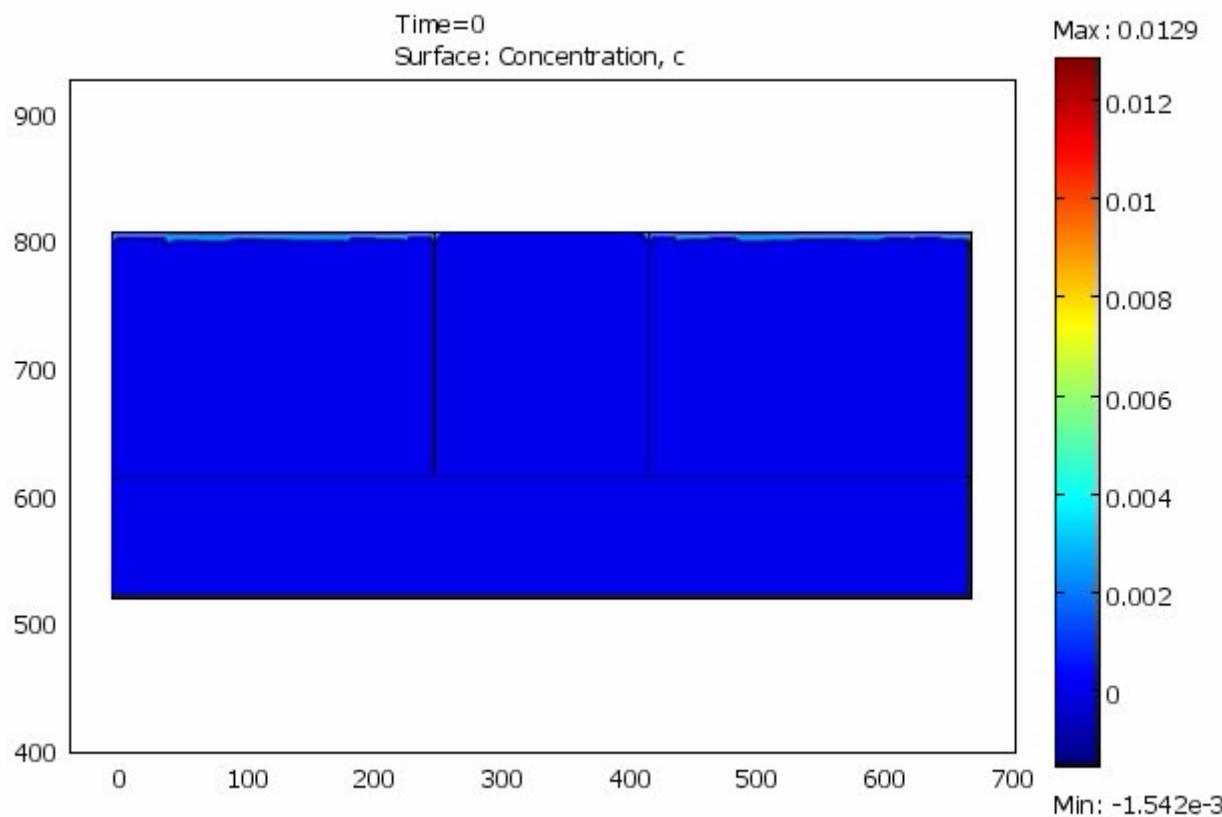
Drogaggio per diffusione



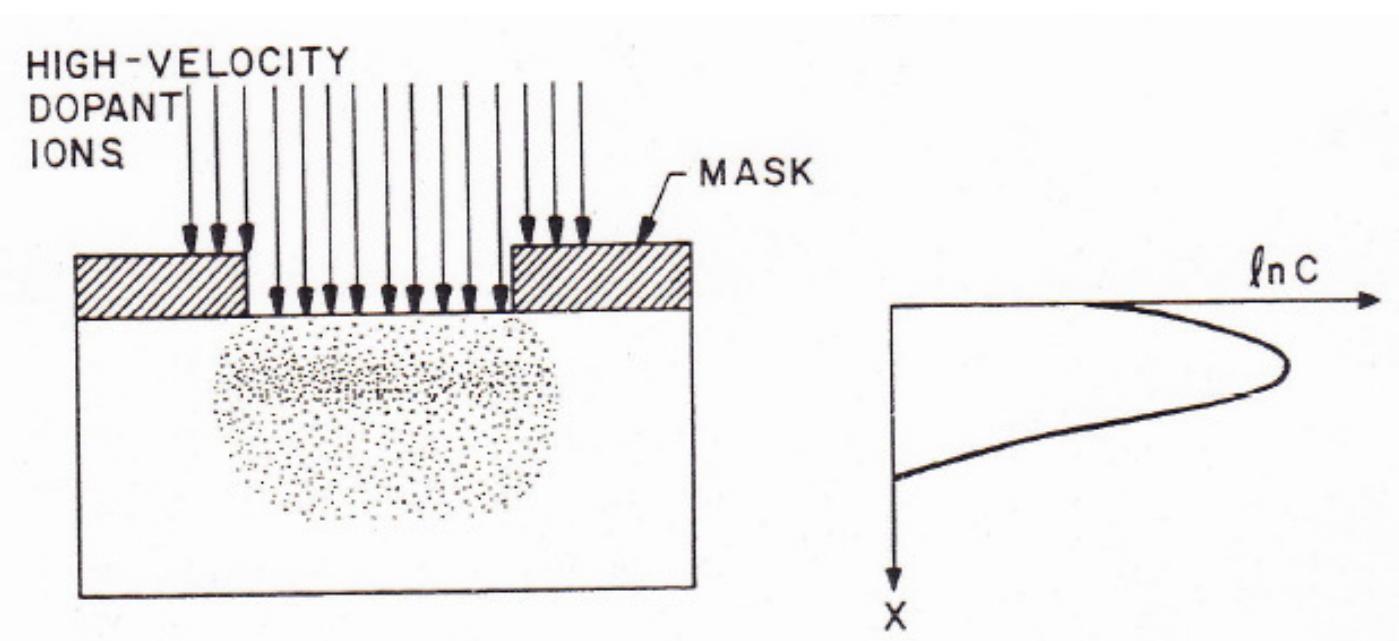
$$\begin{aligned} J &= -D_A^* \cdot \text{grad } C_A \\ D_A^* &= D_{AI} \cdot \left(\frac{C_{AI}}{C_A} \right) + D_{AV} \cdot \left(\frac{C_{AV}}{C_A} \right) = \\ &= D_A^0 \cdot \exp \left(-\frac{E_A^0}{k \cdot T} \right) \end{aligned}$$

Figure 3.1-4: Intrinsic diffusion coefficients for the most common diffusers in silicon.

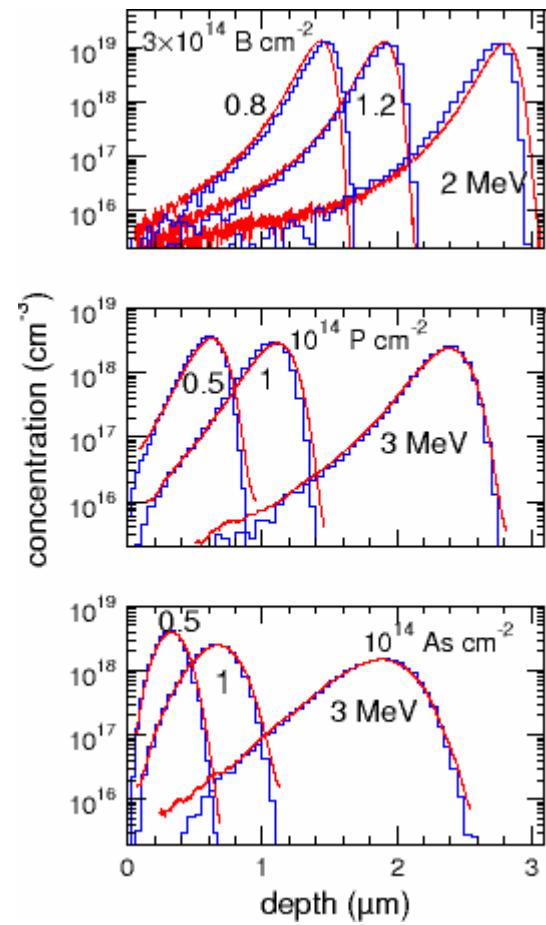
Drogaggio per diffusione



Drogaggio per impiantazione



Drogaggio per impiantazione



Drogaggio per impiantazione Channeling

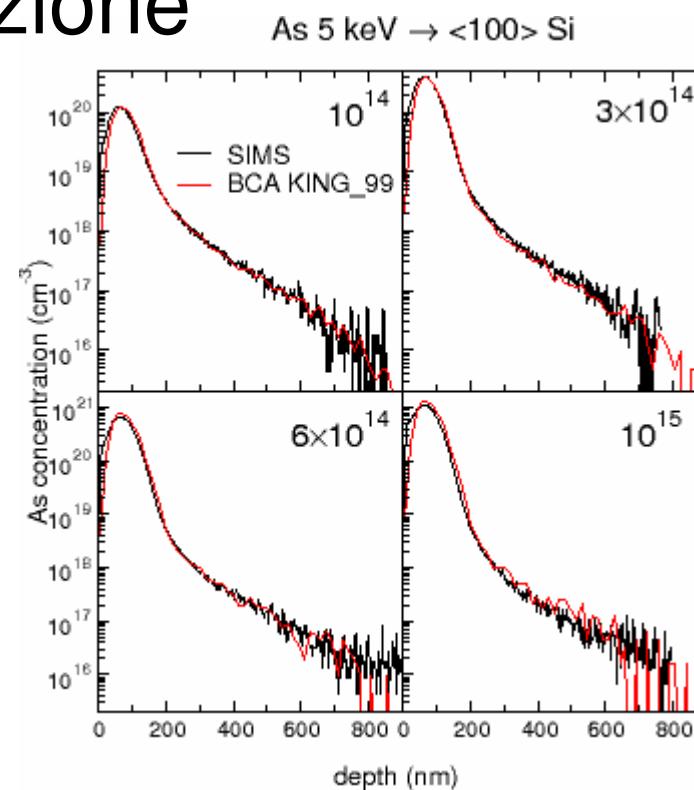
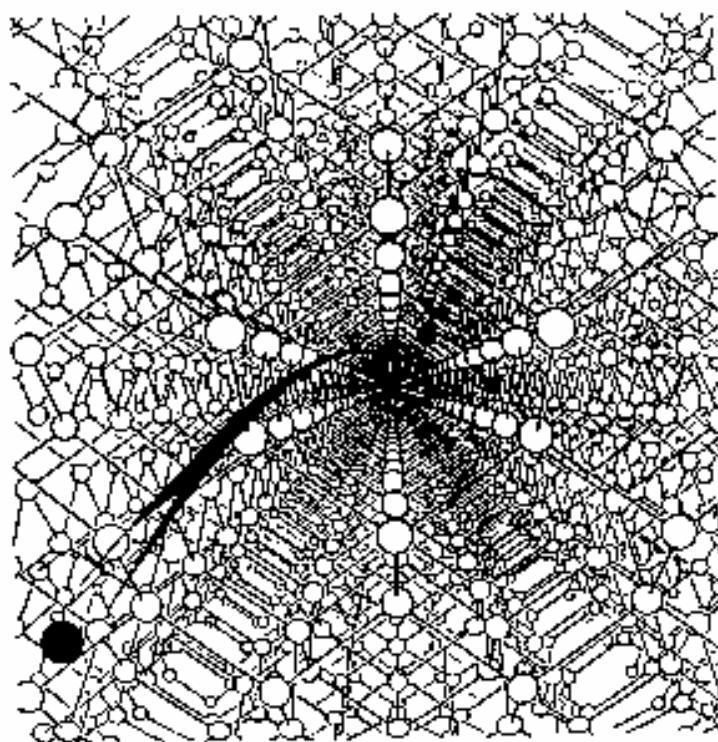
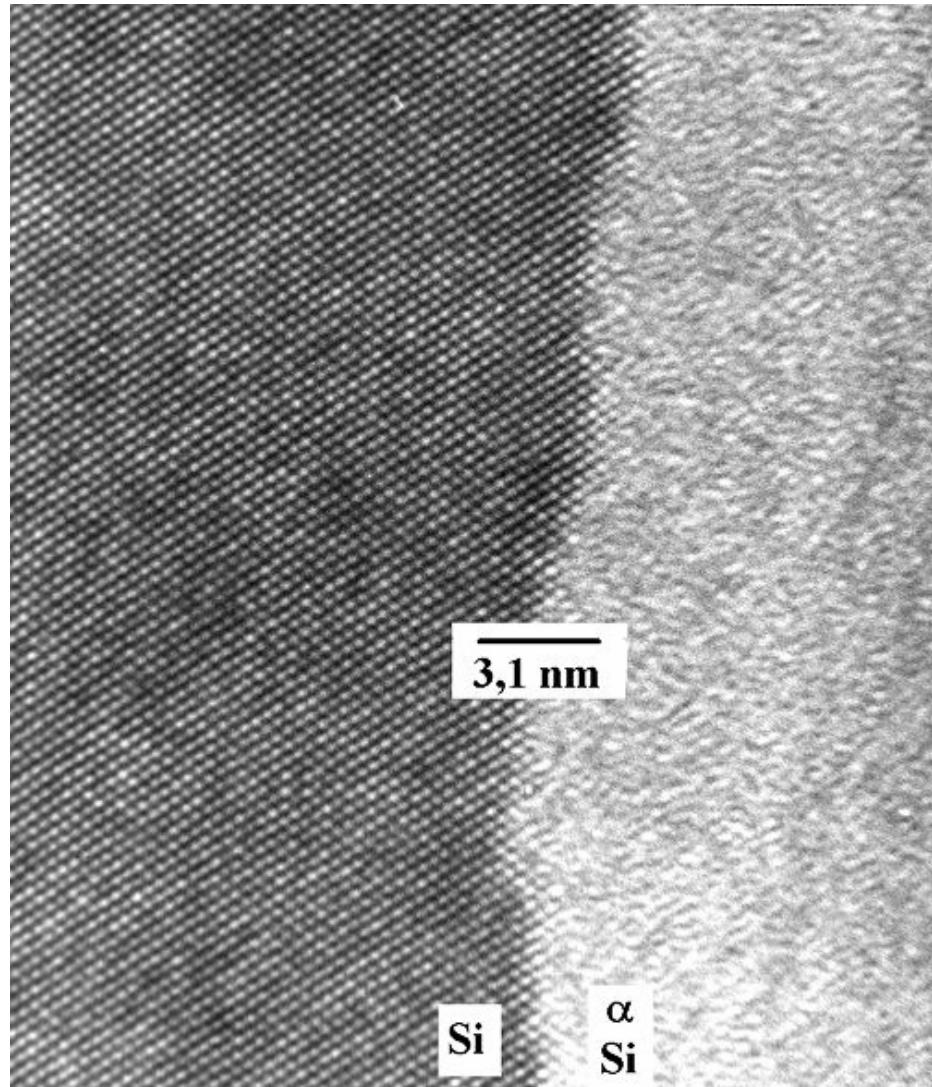


Fig. 2.2: Comparison of measured (SIMS) (black) and simulated (red) depth distribution profiles of 5 keV As ions implanted in Si at different implantation fluences under <100> channeling orientation. Long penetrating tails due to channeling, evident in the experimental profiles, are reproduced with very good accuracy by MC-BCA simulation

Drogaggio per impiantazione Damage



Drogaggio per impiantazione Annealing

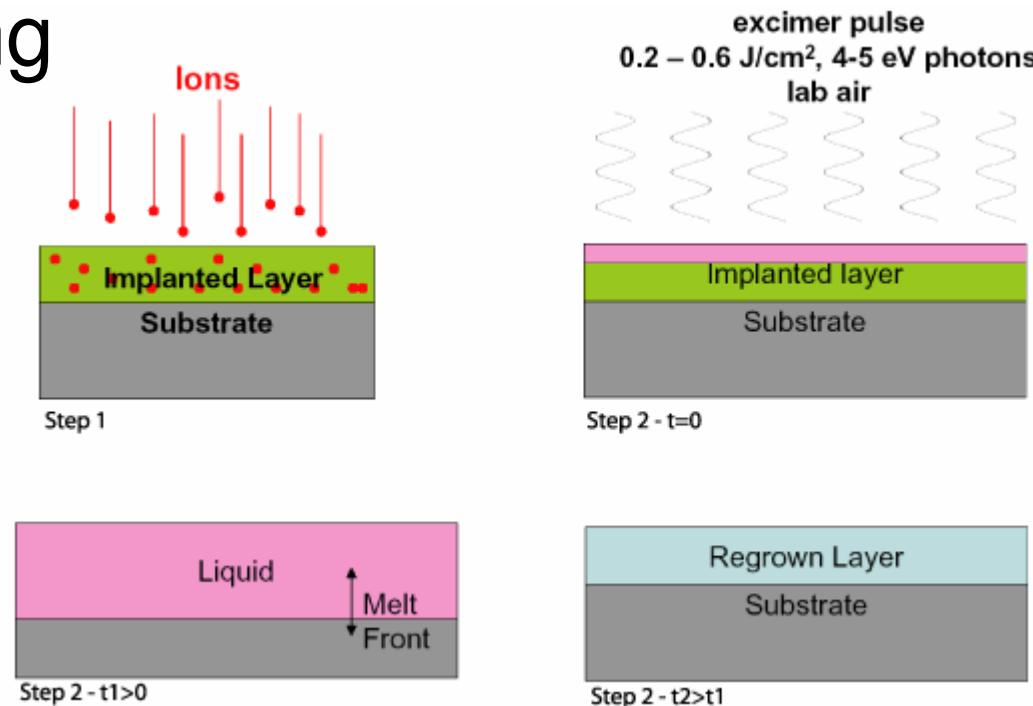
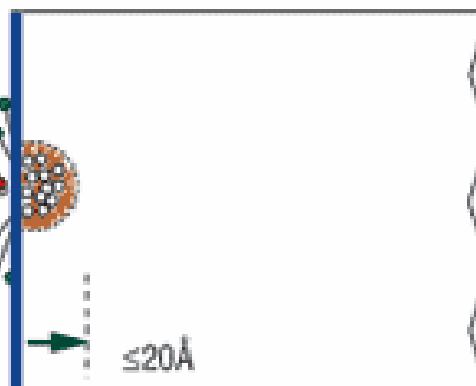
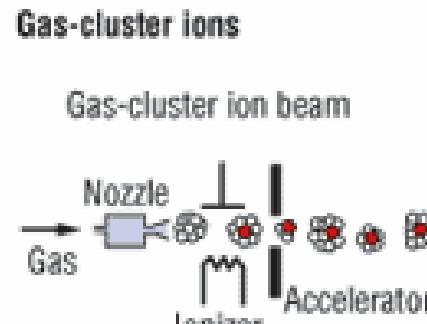
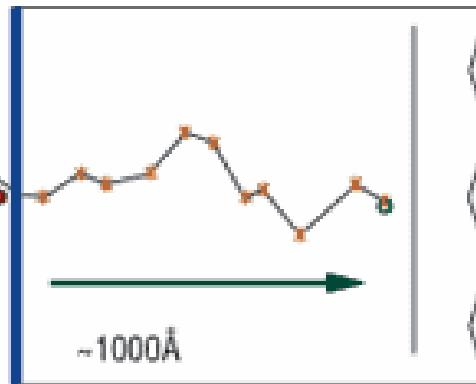
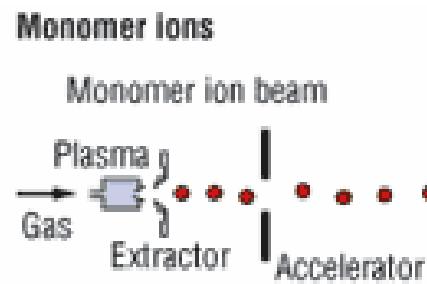


Figure 1 - Schematic of the ion implantation and pulsed-laser melting (II-PLM) process used by our group to synthesize semiconductor alloy films. A semiconductor wafer is first implanted with the alloying species and then irradiated with a single pulse from an excimer laser. The laser energy is converted to heat, which melts through the implant-damaged layer into the underlying substrate. Epitaxial solidification proceeds as heat is extracted into the substrate, resulting in a single-crystalline alloy film on the original substrate.

Drogaggio per infusione



B_2H_6

