Fig. 10 Variation of depletion layer width and output characteristics of a JFET under various biasing conditions. (a) $V_G = 0$ and small V_D. (b) $V_G = 0$ and at pinch-off. (c) $V_G = 0$ and post pinch-off ($V_D > V_{D\,sat}$). (d) $V_G = -1$ V and small V_D.

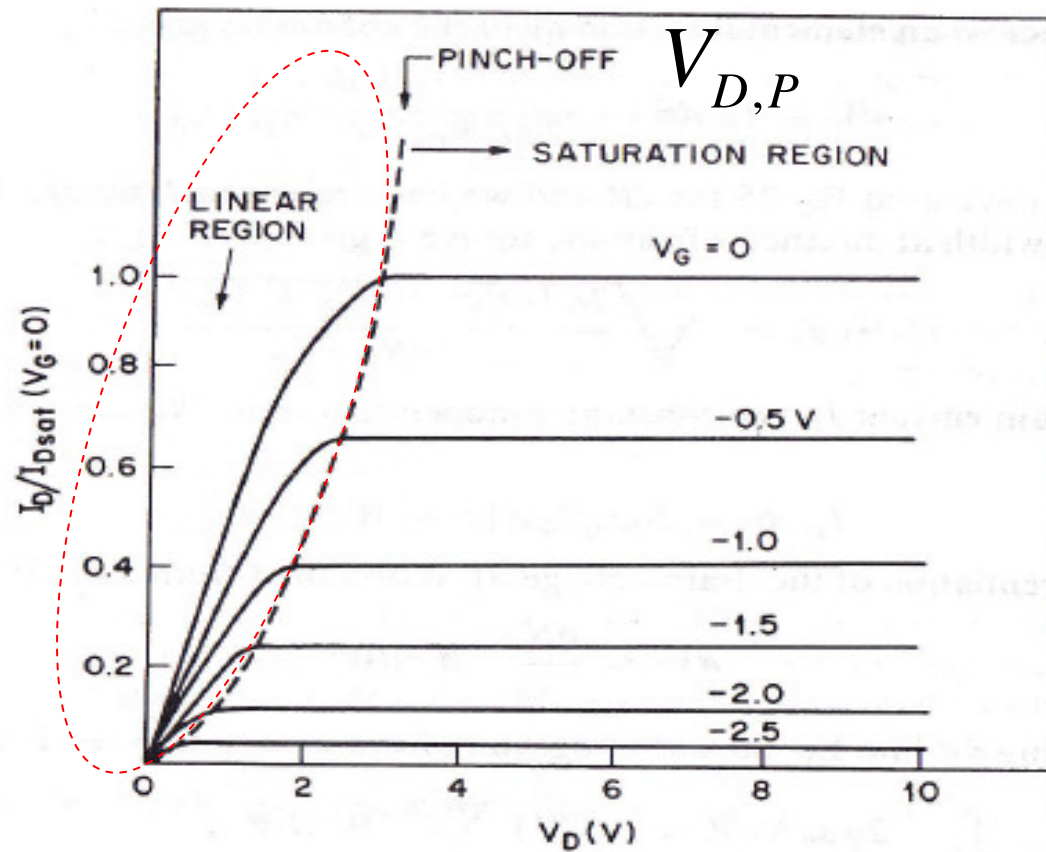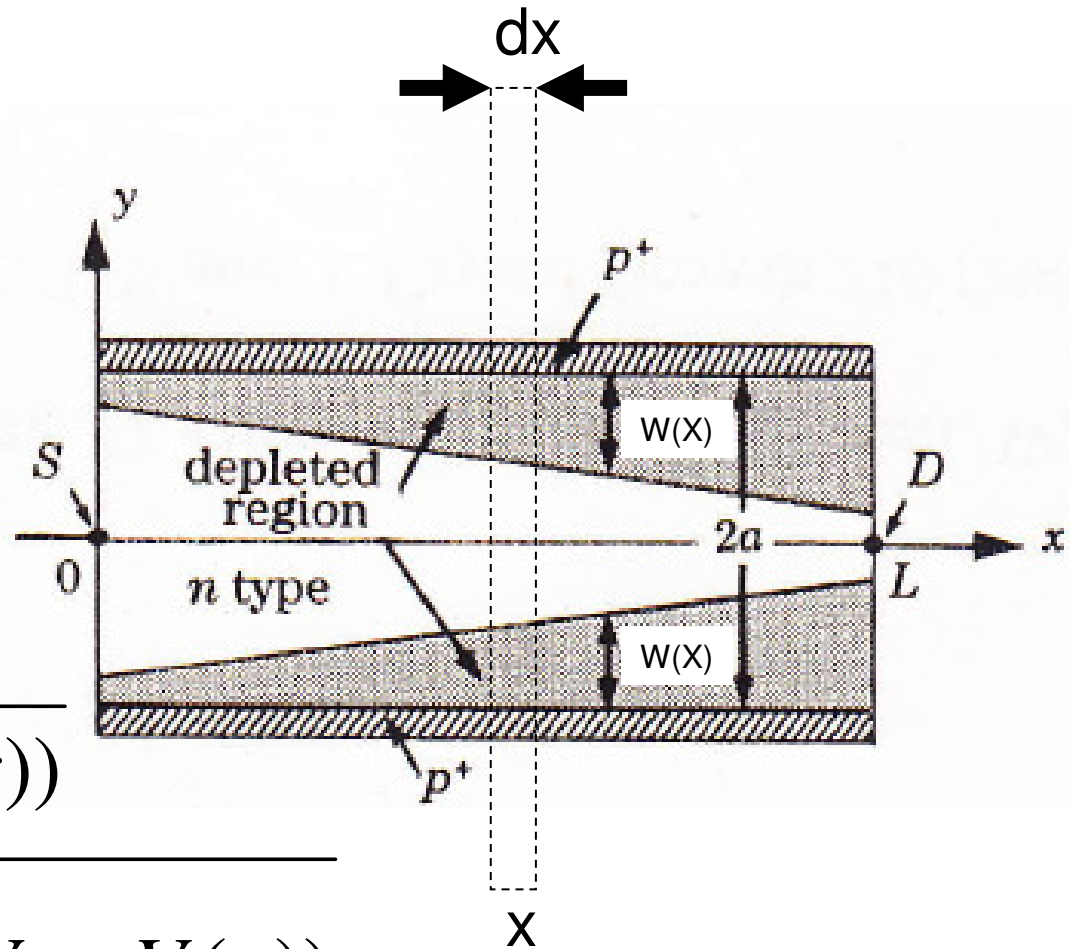# JFET: caratteristiche statiche

Fig. 12   Normalized ideal current–voltage characteristics with $V_P = 3.2$ V.

JFET

$$dV(x) = I_D dR(x)$$

$$dR(x) = \frac{dx}{\sigma b 2(a - W(x))}$$

$$W(x) = \sqrt{\frac{2\varepsilon}{qN_D}(V_{bi} - V_G + V(x))}$$

Linear region

$$\boxed{V_D \le V_{D,P} = \Psi + V_G - V_{bi}}$$

JFET

$$\Psi = \frac{qN_D}{2\varepsilon a^2}$$

$$dV(x)\sigma b2a\left(1 - \sqrt{\frac{V_{bi} - V_G + V(x)}{\Psi}}\right) = I_D dx$$

$$\int_0^{V_D} dV(x)\sigma b2a\left(1 - \sqrt{\frac{V_{bi} - V_G + V(x)}{\Psi}}\right) = \int_0^L I_D dx$$

$$I_D = \frac{\sigma b2a}{L}\left(V_D - \frac{2}{3}\sqrt{\frac{1}{\Psi}}\left[(V_{bi} - V_G + V_D)^{3/2} - (V_{bi} - V_G)^{3/2}\right]\right)$$

JFET $\boxed{\Psi = \dfrac{qN_D}{2\varepsilon a^2}}$ $\boxed{V_D \le V_{D,P} = \Psi + V_G - V_{bi}}$

$$I_D = \frac{\sigma b 2a}{L}\left(V_D - \frac{2}{3}\sqrt{\frac{1}{\Psi}}\left[(V_{bi} - V_G + V_D)^{3/2} - (V_{bi} - V_G)^{3/2}\right]\right)$$

$$g_D = \frac{\partial I_D}{\partial V_D} = \frac{\sigma b 2a}{L}\left(1 - \sqrt{\frac{(V_{bi} - V_G + V_D)}{\Psi}}\right) = \frac{\sigma b}{L}2(a - W)$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{\sigma b 2a}{L}\left(\sqrt{\frac{(V_{bi} - V_G + V_D)}{\Psi}} - \sqrt{\frac{(V_{bi} - V_G)}{\Psi}}\right)$$

JFET: caratteristiche statiche
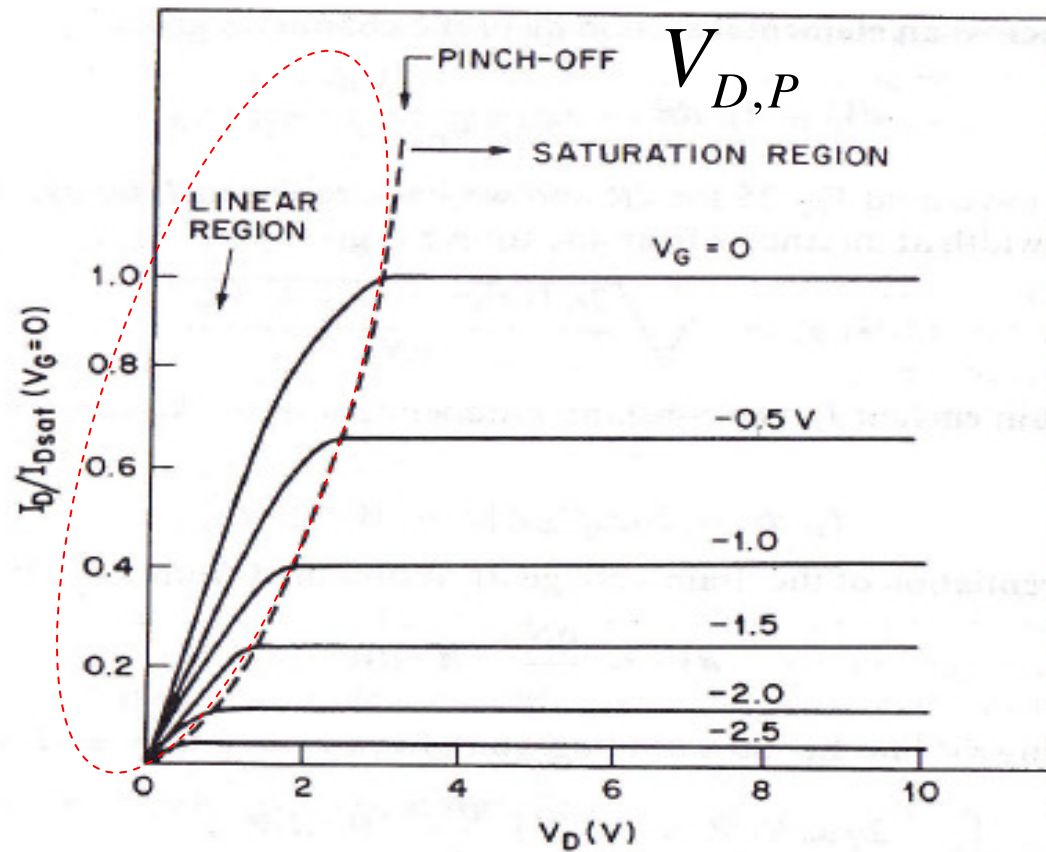
Fig. 12   Normalized ideal current-voltage characteristics with $V_P = 3.2$ V.

JFET

$$V_D = V_{D,P} = \Psi + V_G - V_{b,i}$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{\sigma b 2a}{L}\left(\sqrt{\frac{(V_{bi} - V_G + V_D)}{\Psi}} - \sqrt{\frac{(V_{bi} - V_G)}{\Psi}}\right)$$

$$g_{m,sat} = \frac{\sigma b 2a}{L}\left(1 - \sqrt{\frac{(V_{bi} - V_G)}{\Psi}}\right) = g_{D,lin}$$

JFET: confronto modello dati
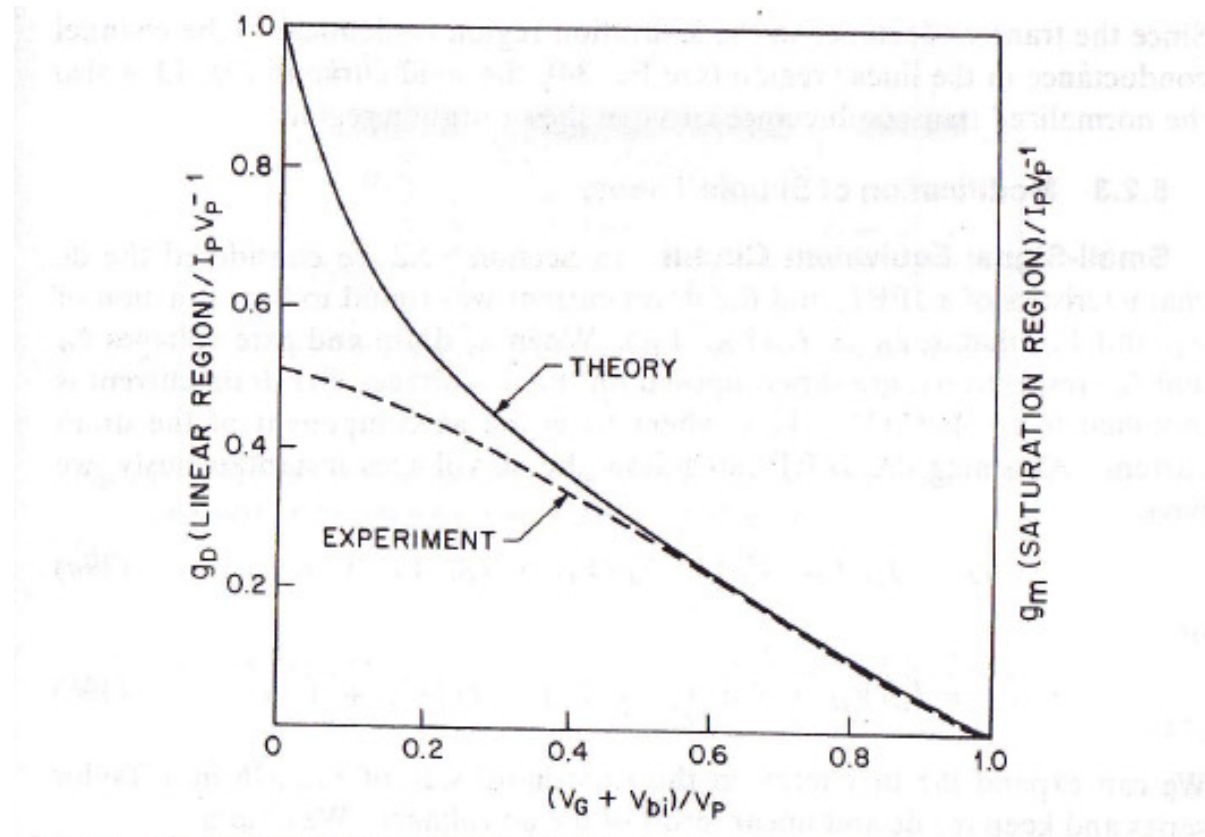
Fig. 13 Normalized drain conductance in the linear region and normalized transconductance in the saturation region versus normalized gate voltage. Solid line is for the ideal case; dotted line is for a practical device having series resistances.

JFET: comportamento dinamico
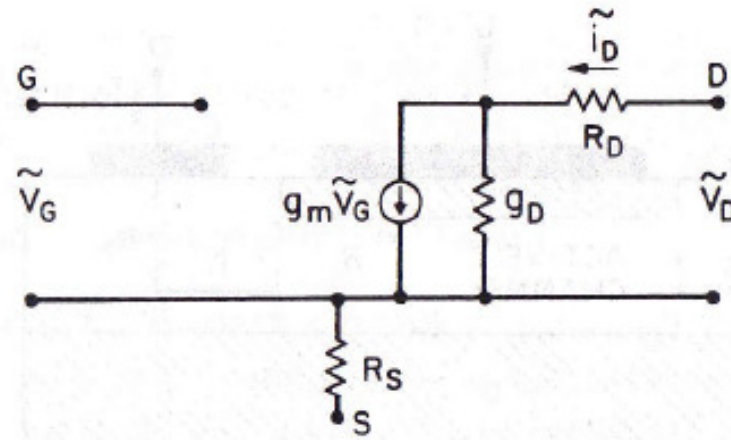
(a) LOW f

JFET: comportamento dinamico
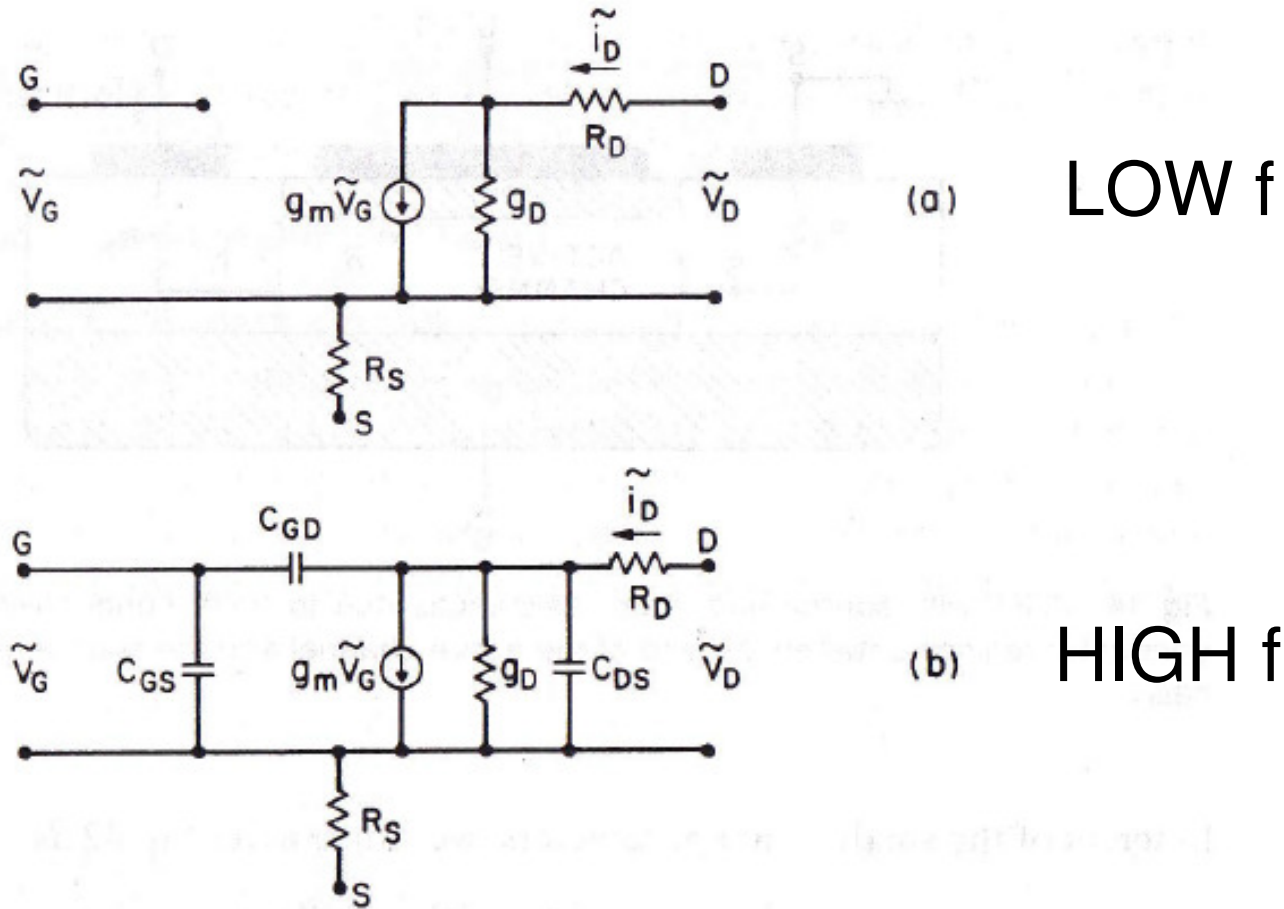
Fig. 15 (a) Low-frequency, small-signal equivalent circuit of the JFET. (b) High-frequency, small-signal equivalent circuit of the JFET.

Diodo MIS
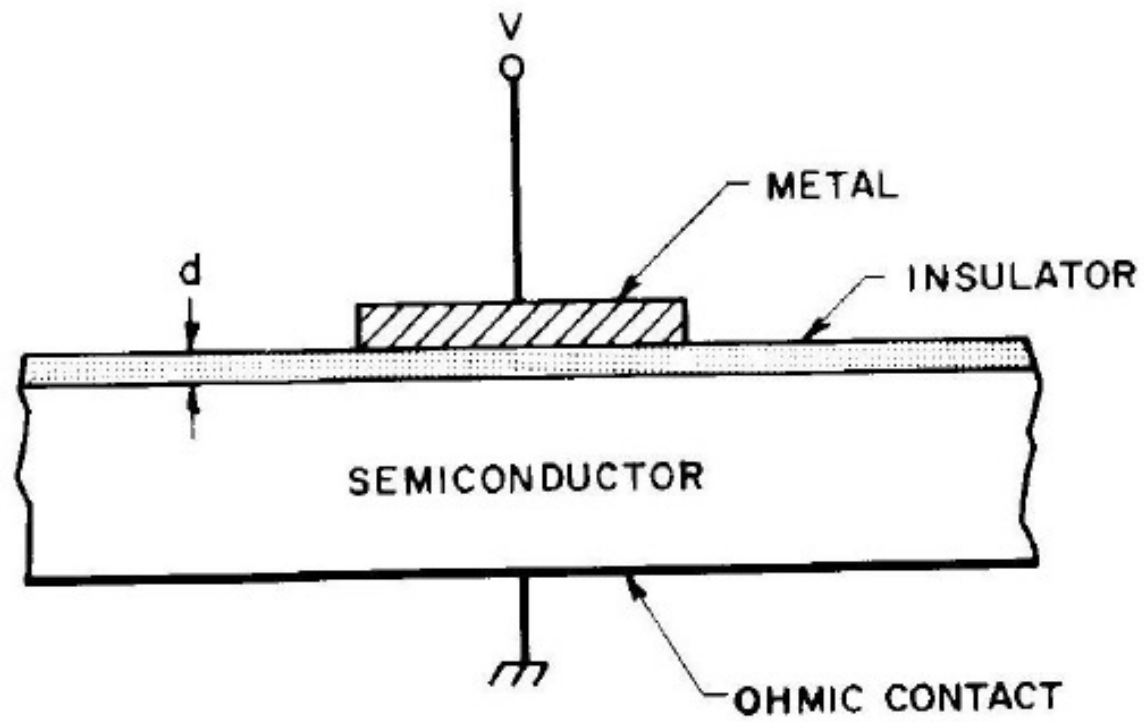
Diodo MIS
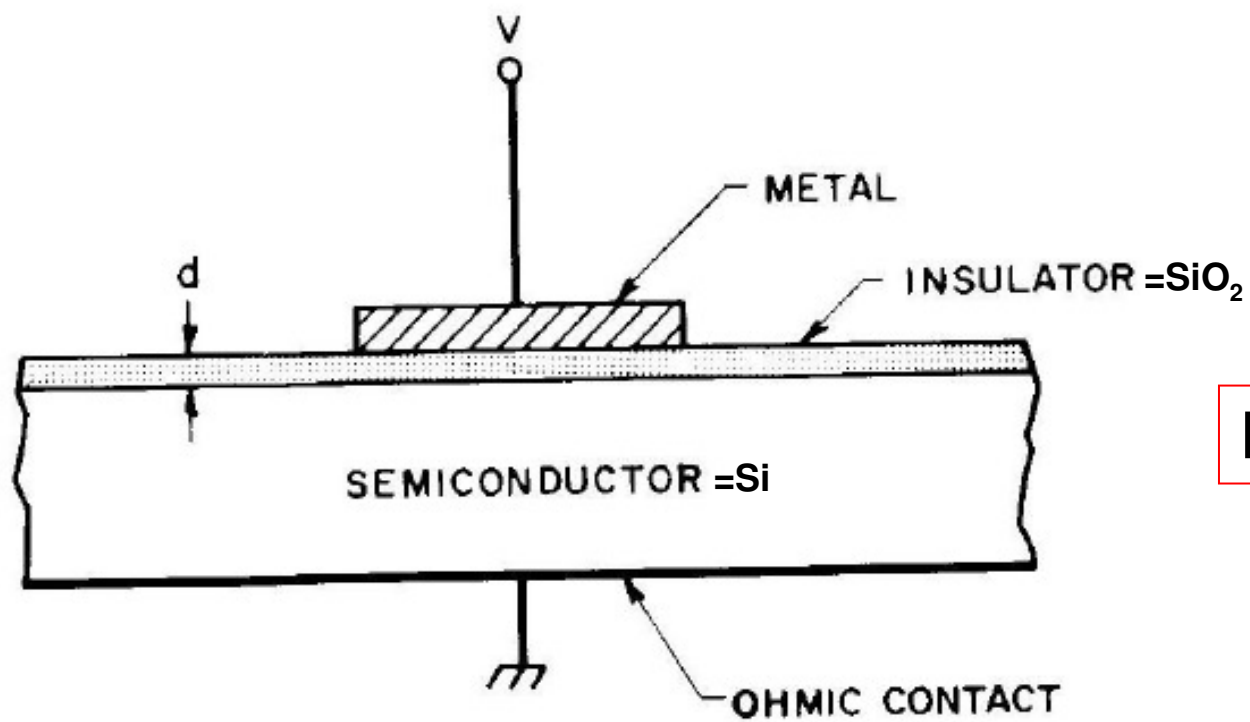
Diodo MOS

Diodo MOS
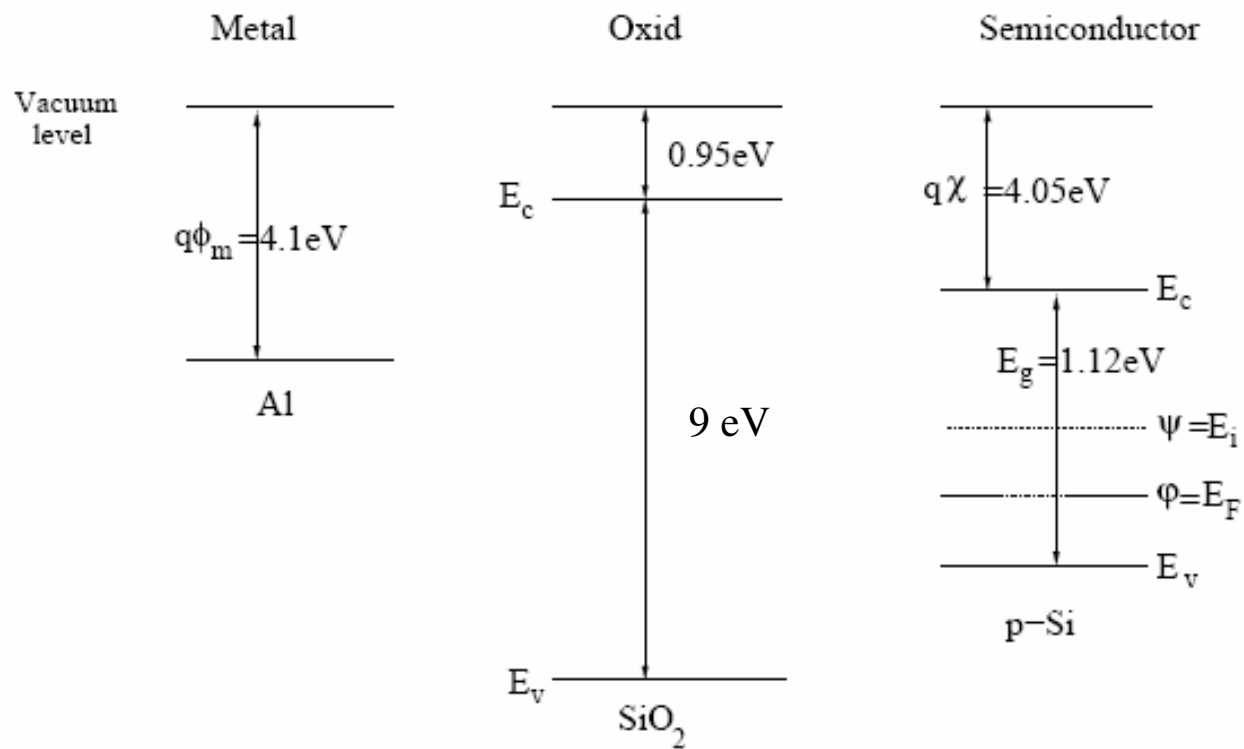
Diodo MOS
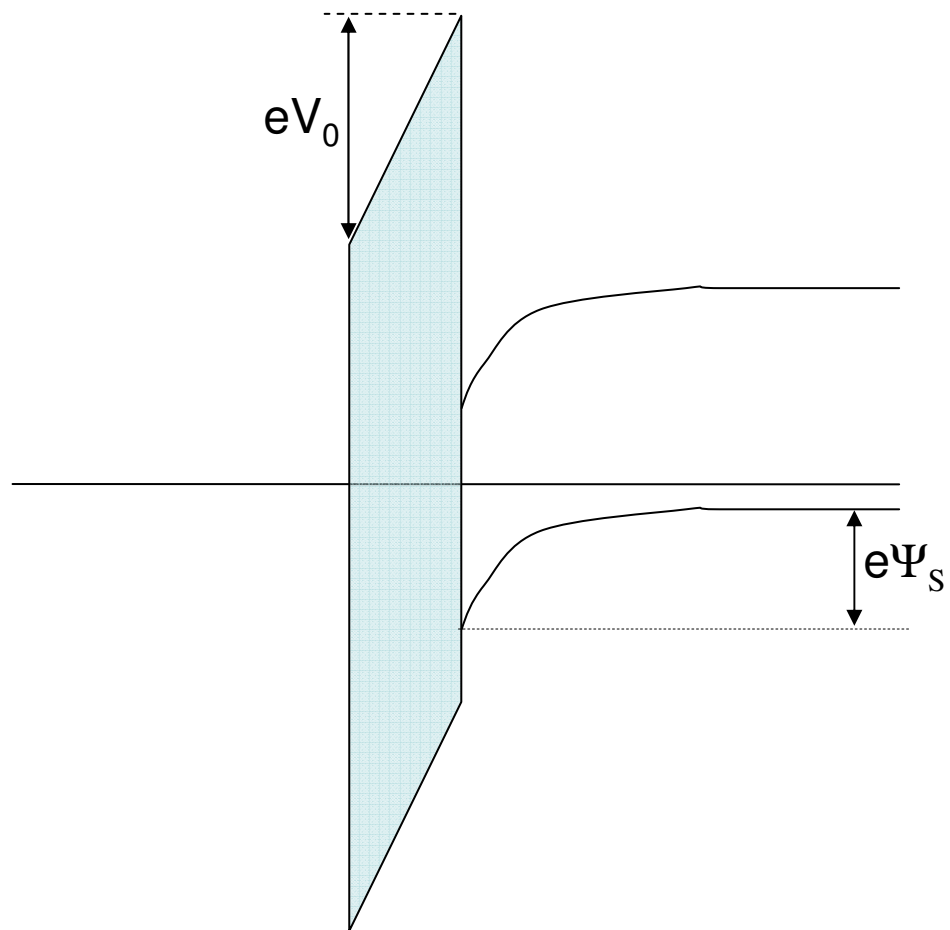
Diodo p-MOS

V=0

Diodo p-MOS

V=0

V>0

V

METAL

INSULATOR

d

SEMICONDUCTOR

OHMIC CONTACT

Diodo p-MOS

V O
METAL
INSULATOR
d
SEMICONDUCTOR
OHMIC CONTACT

V=0

V>0
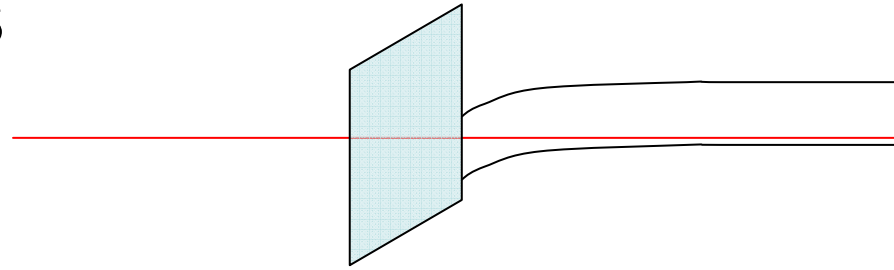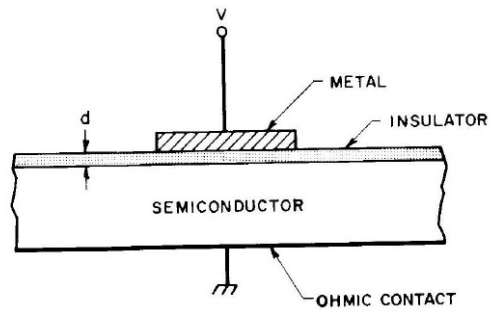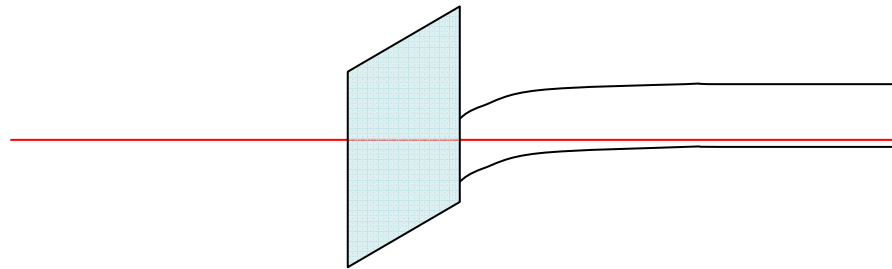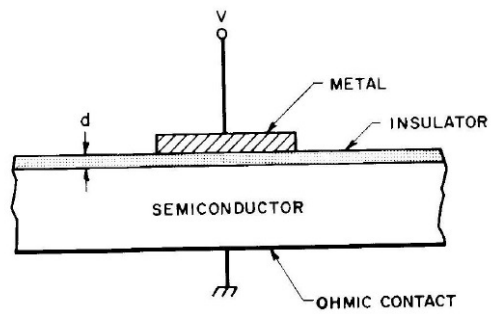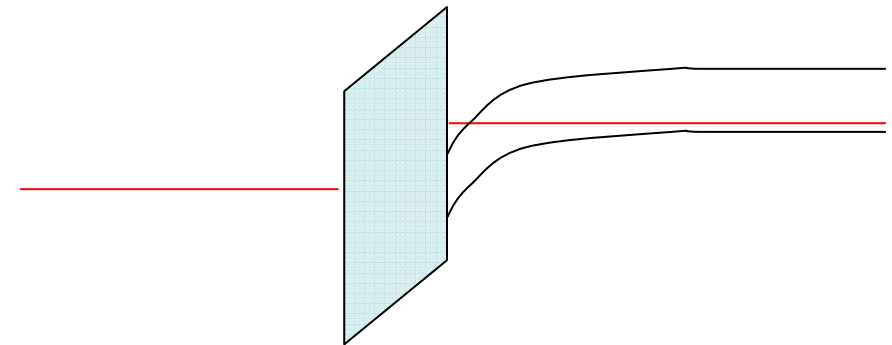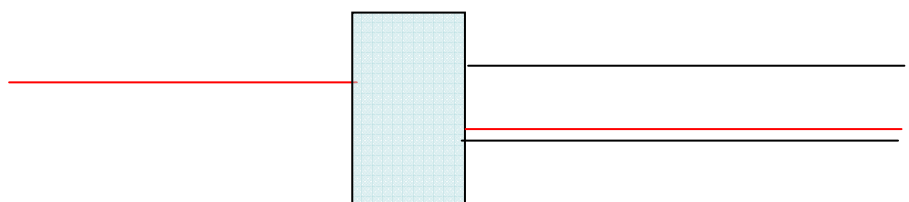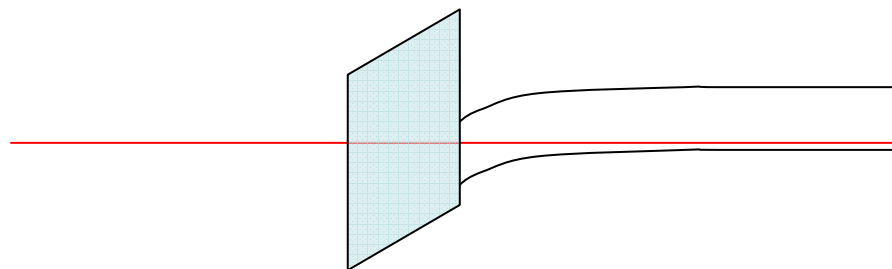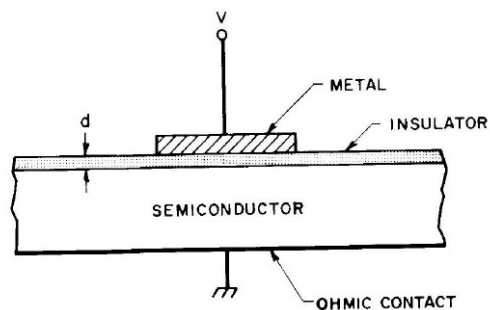
$V=-V_0- \Psi_S$

Diodo p-MOS

V=0
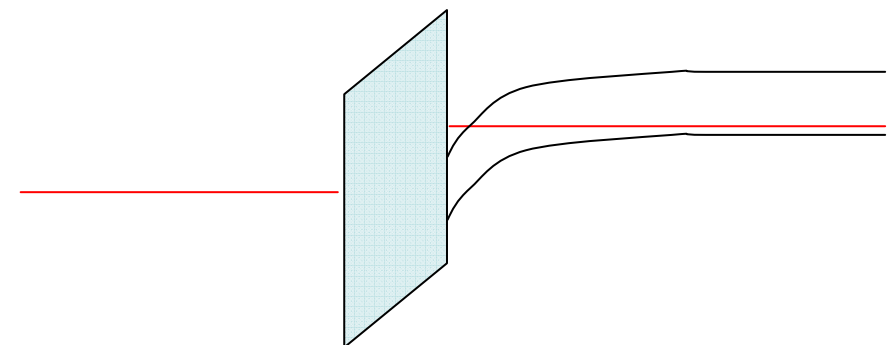
V>0
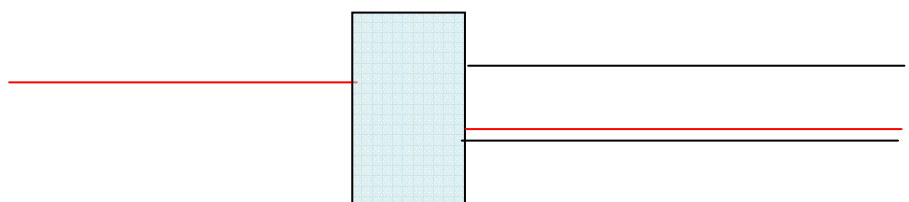
$V = -V_0 - \Psi_S$
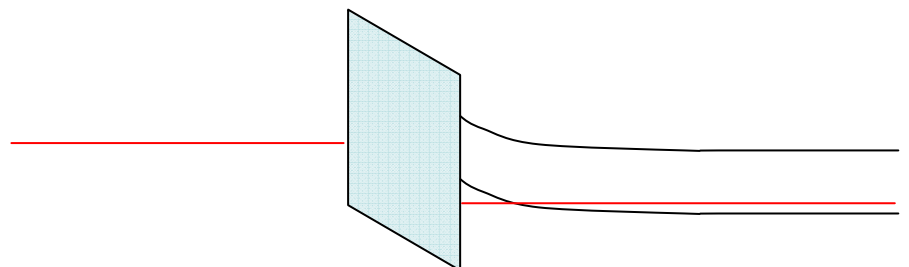
$V < -V_0 - \Psi_S$

Diodo p-MOS

Svuotamento
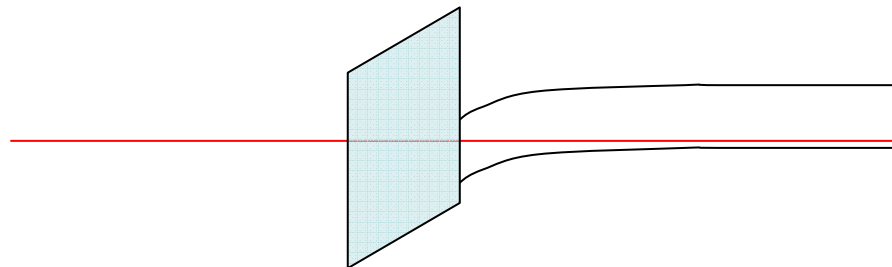
$V=0$

Inversione
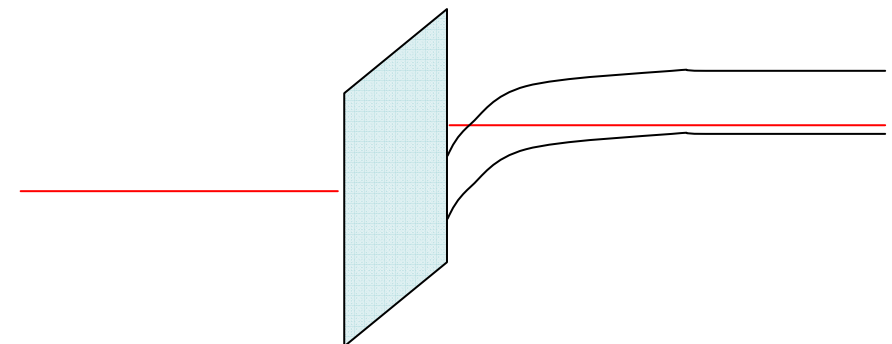
$V>0$

Non polarizzato
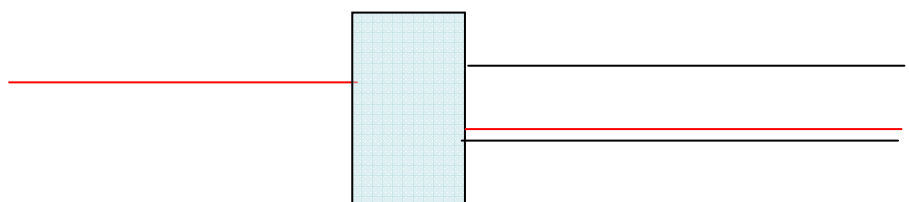
$V=-V_0-\Psi_S$

Accumulo
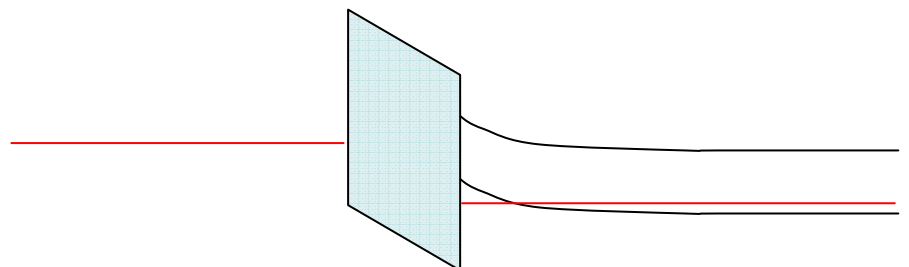
$V<-V_0-\Psi_S$

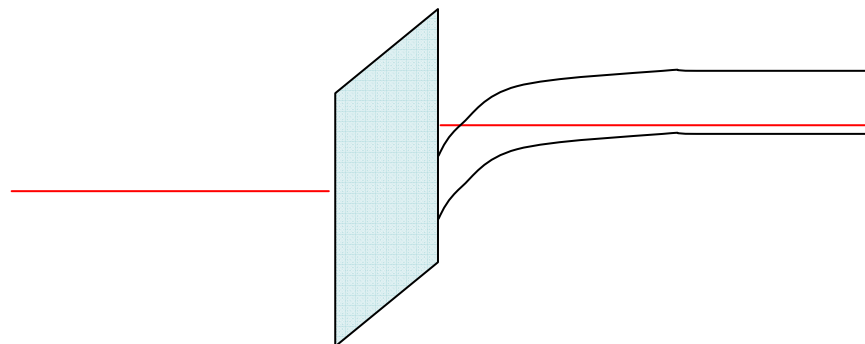# Diodo p-MOS
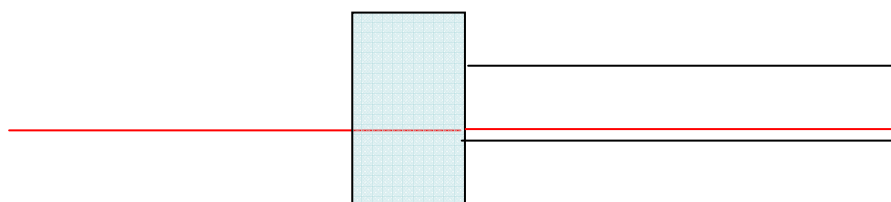
Svuotamento

$V_T > V > 0$

Inversione

$V > V_T$

Non polarizzato

$V = 0$

Accumulo

$V < 0$
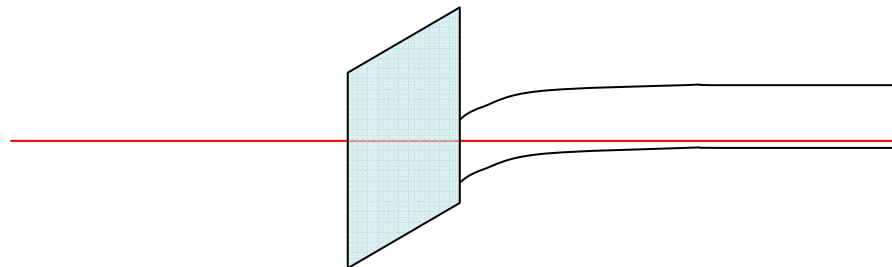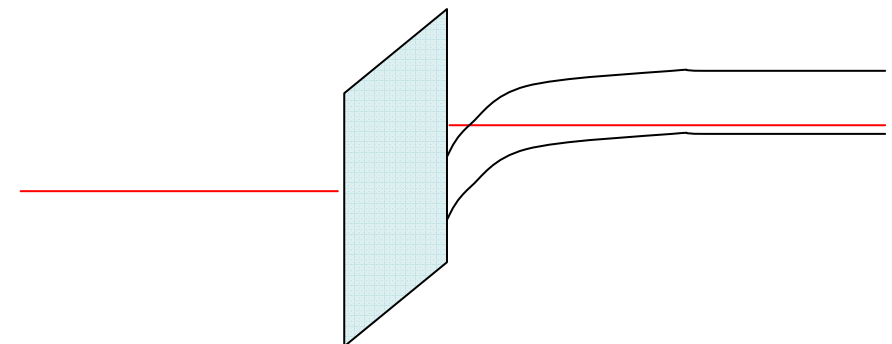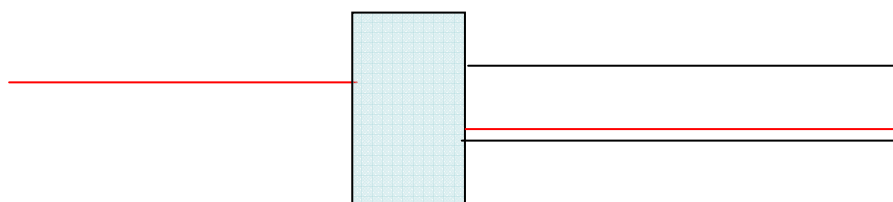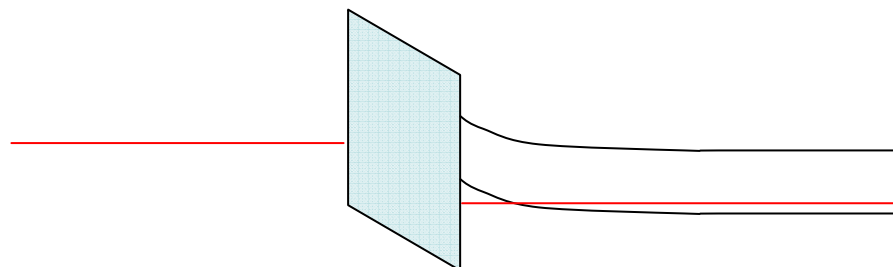
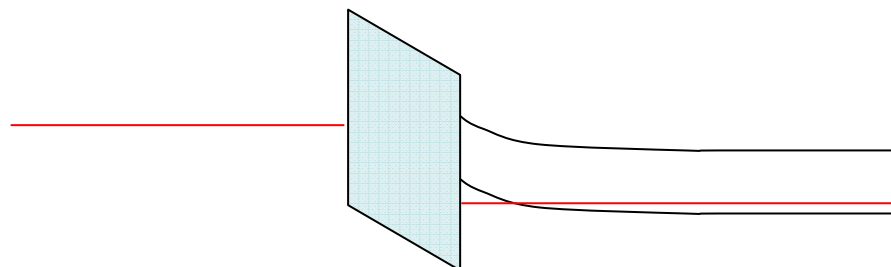# Diodo p-MOS Ideale

Svuotamento

$V_T > V > 0$

Inversione

$V > V_T$

Non polarizzato

$V = 0$
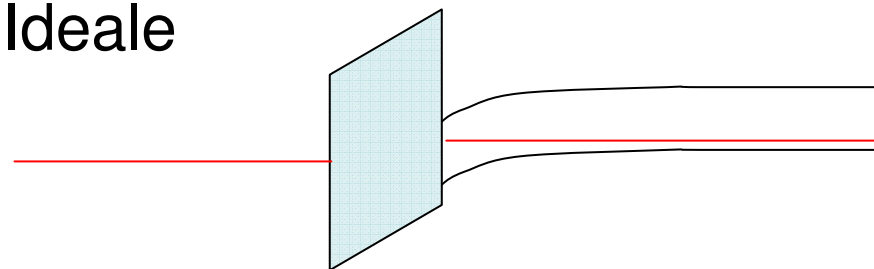
Accumulo

$V < 0$
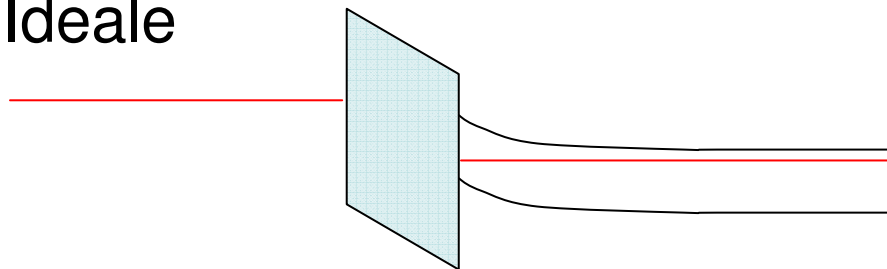
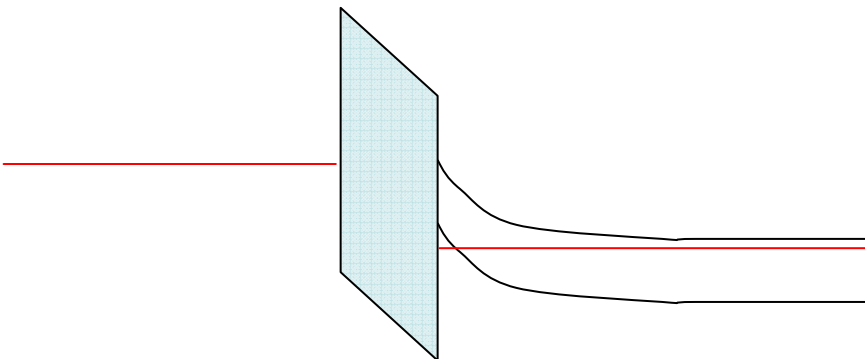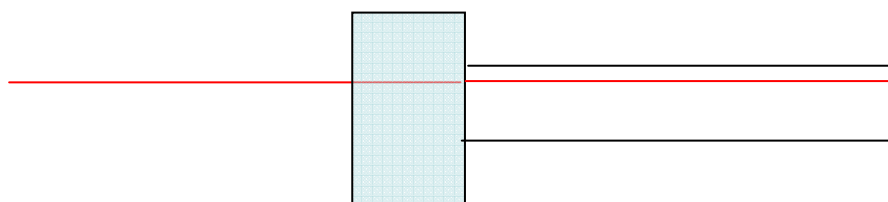# Diodo n-MOS Ideale

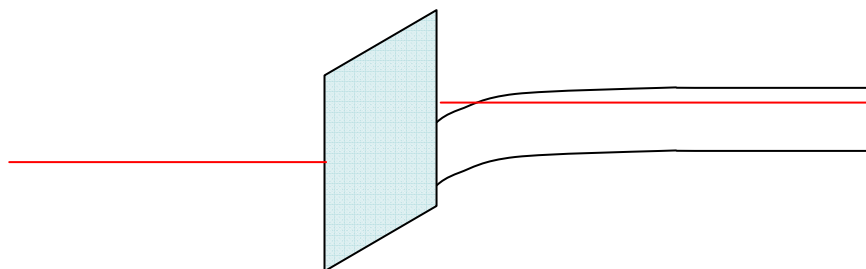Svuotamento

$0 > V > -V_T$

Inversione

$V < -V_T$

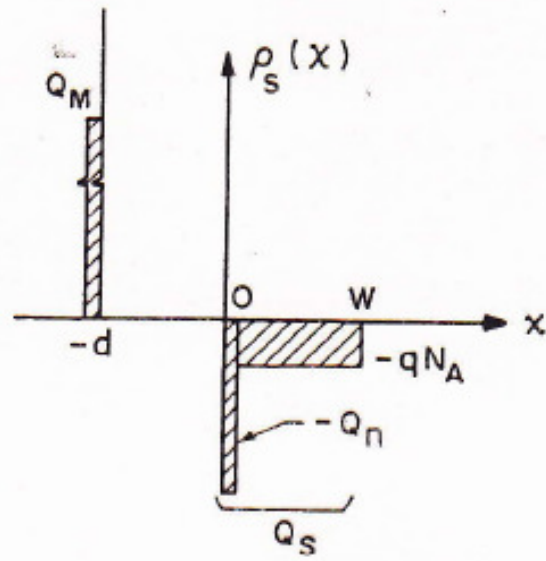Non polarizzato
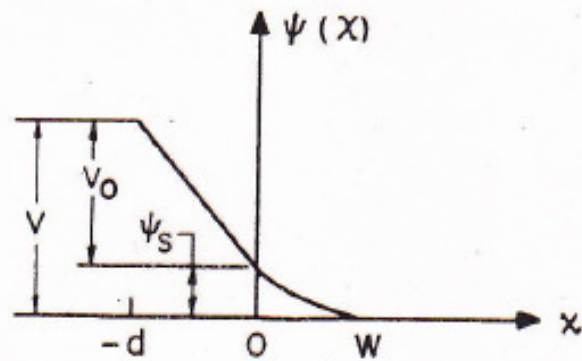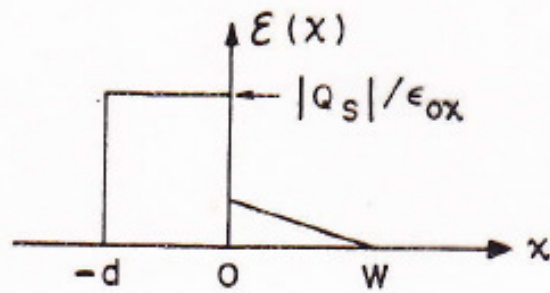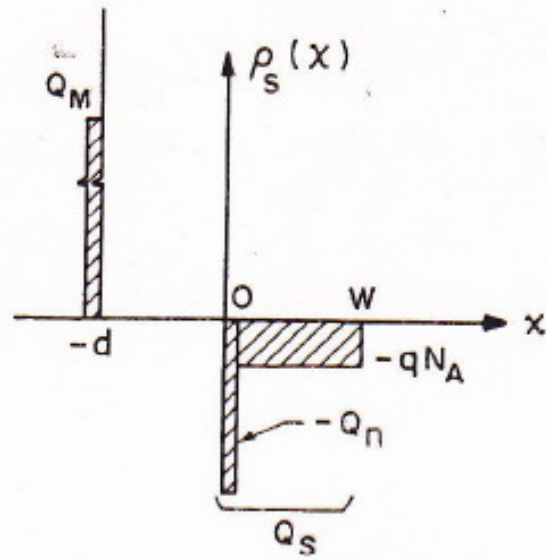
$V = 0$

Accumulo

$V > 0$

Diodo p-MOS Ideale
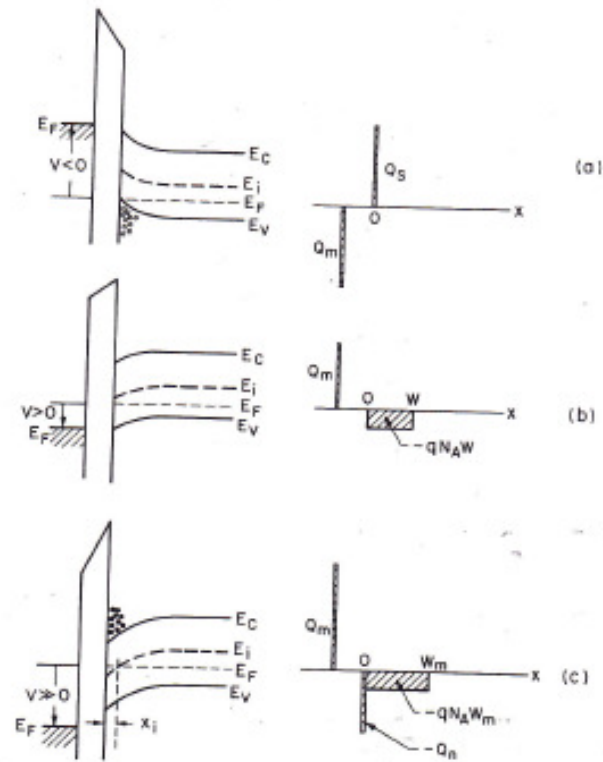
Fig. 23 Energy band diagrams and charge distributions of an ideal MOS diode (a) Accumulation. (b) Depletion. (c) Inversion.

(b)

(b)

(c)

(d)

Varactor