BJT distribuzione portatori minoritari

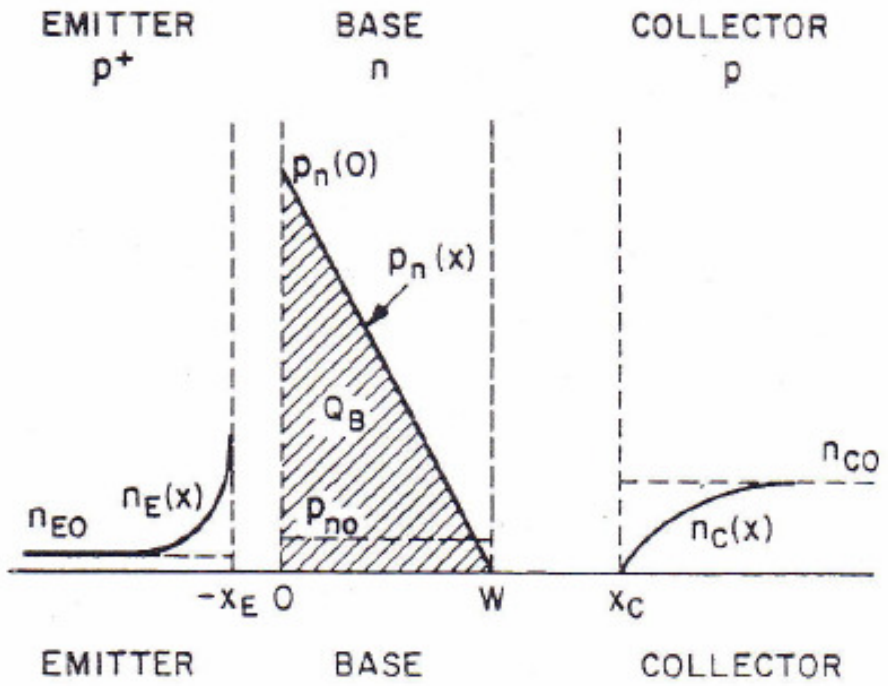
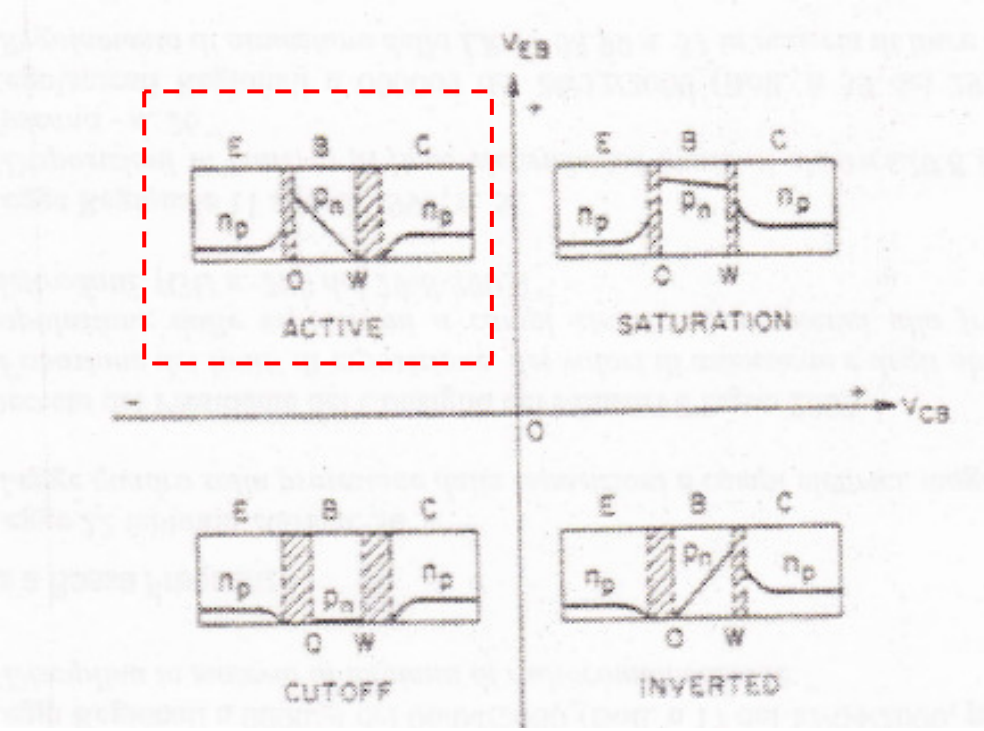


Fig. 7 Minority carrier distributions in various regions of a *p–n–p* transistor under active mode of operation.

Distribuzione portatori minoritari



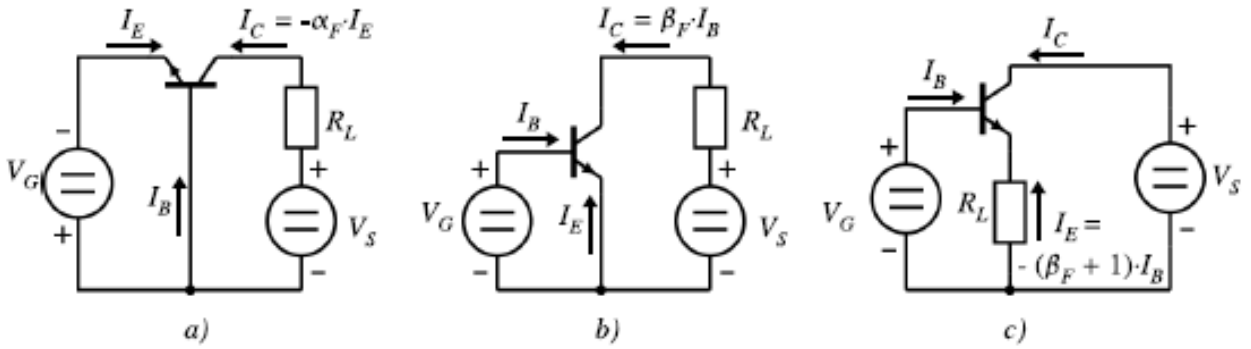
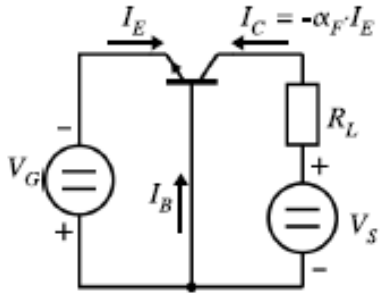
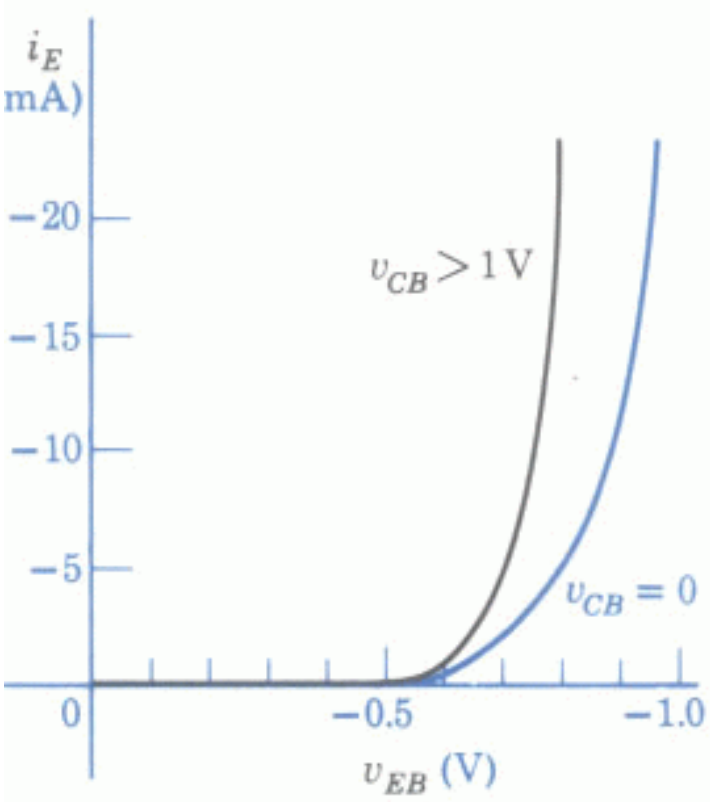


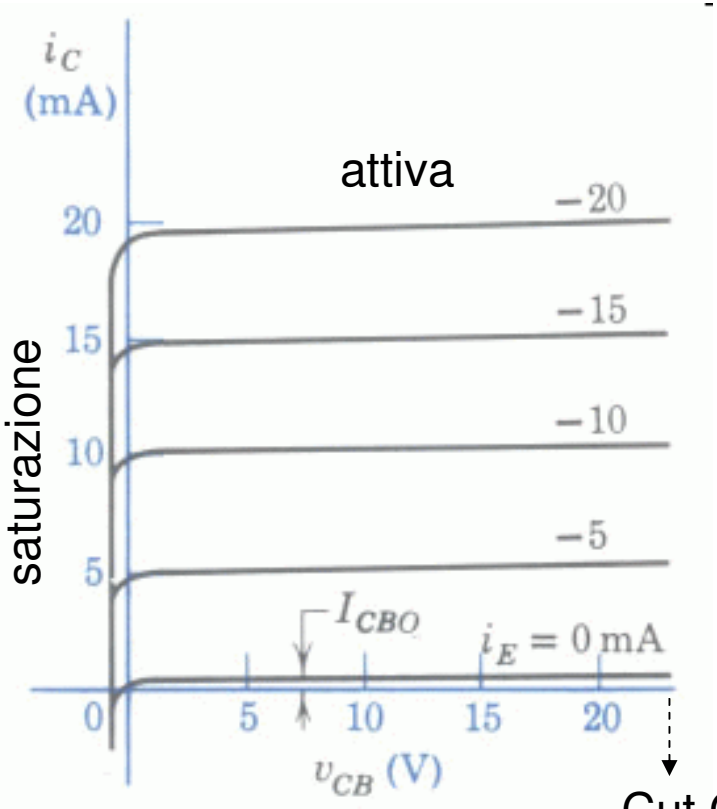
Figura 4.4: Configurazioni di utilizzo del transistor bjt: *a*) base comune; *b*) emettitore comune; *c*) collettore comune.

Base Comune



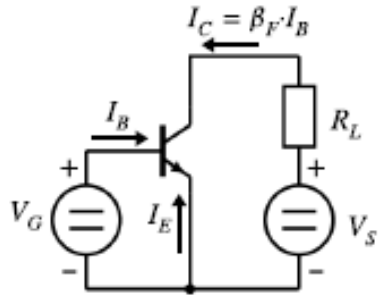


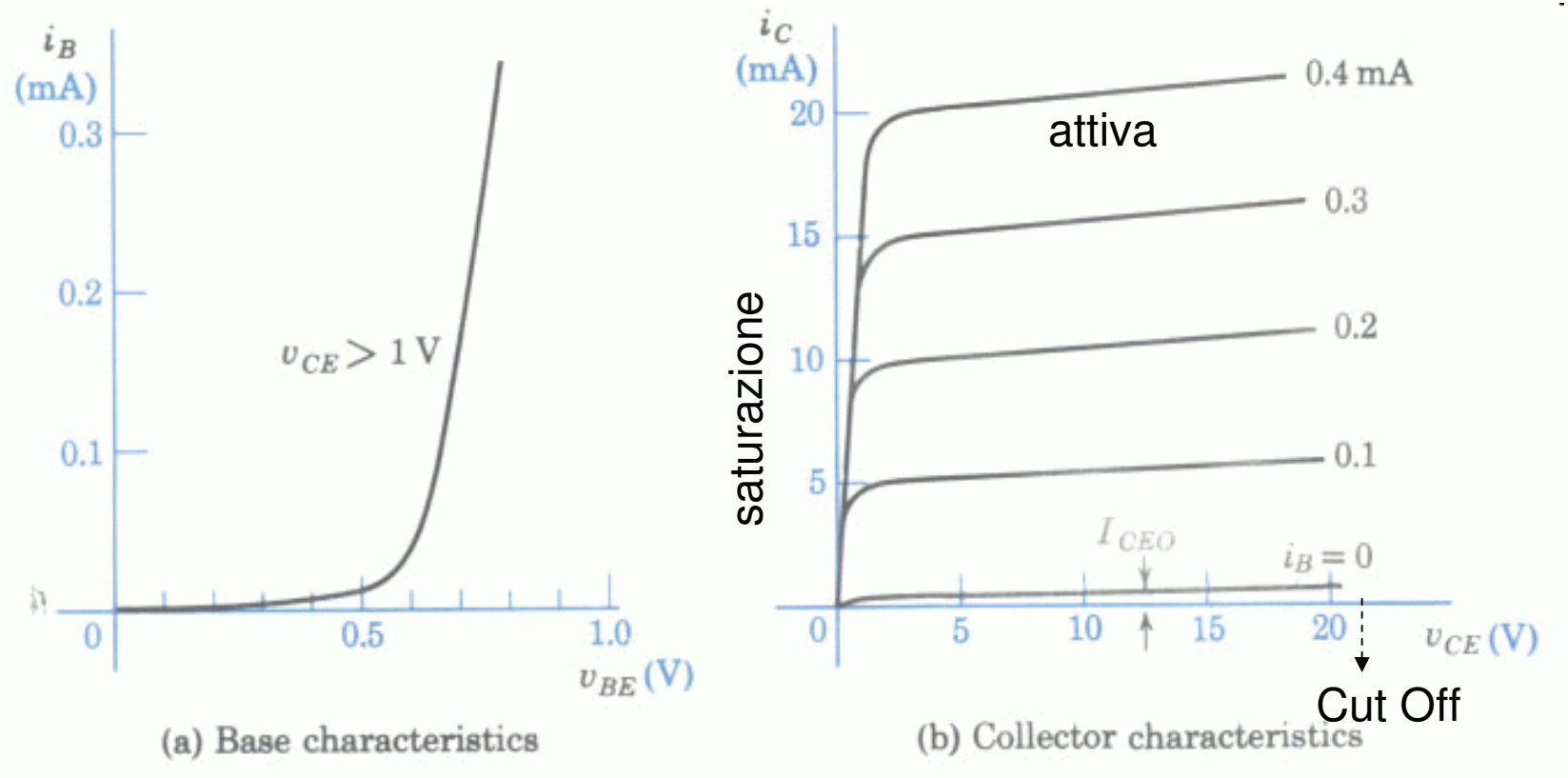
(b) Emitter characteristics



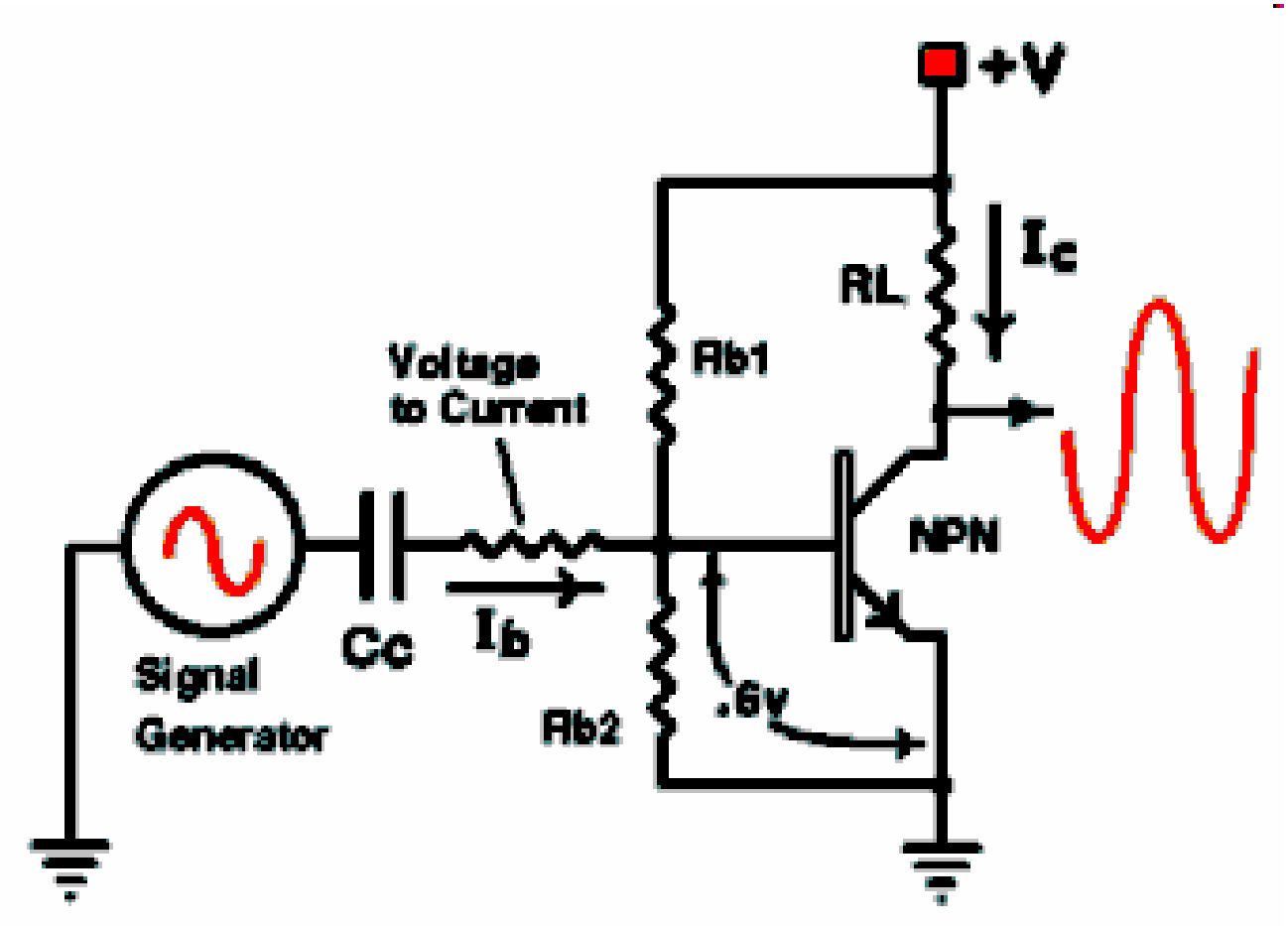
(c) Collector characteristics

Emettitore Comune

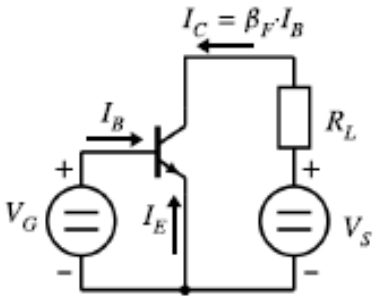




Amplificatore di tensione e/o corrente



Emettitore Comune

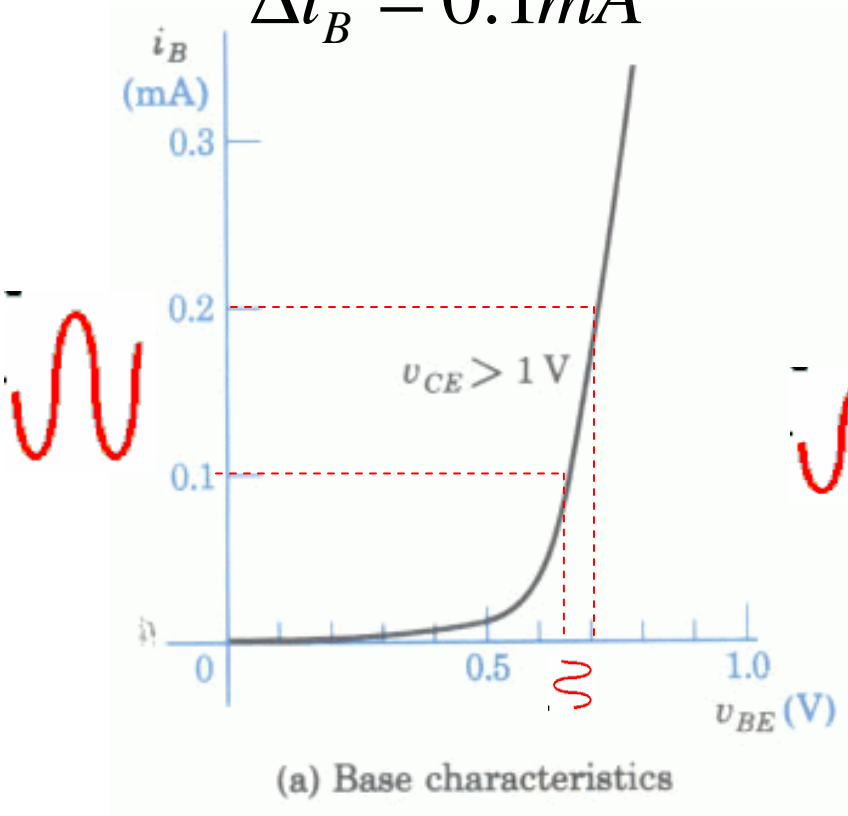


$$\Delta V_{BE} = 0.07V$$

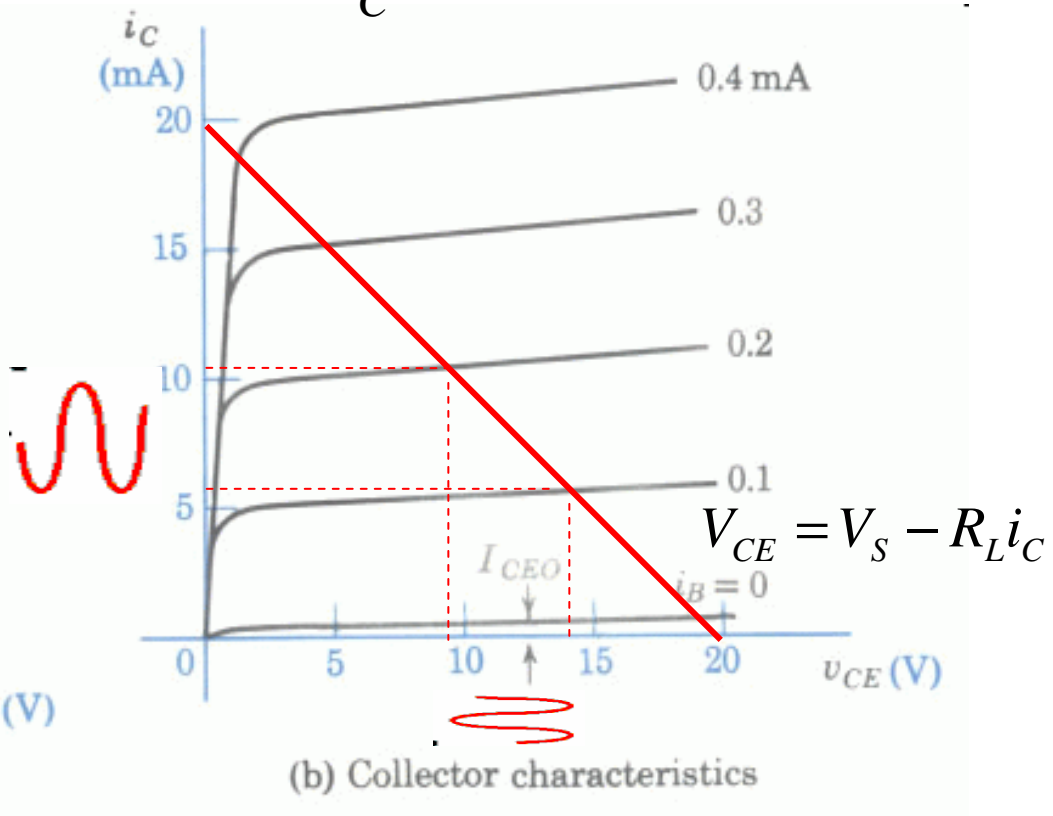
$$\Delta i_B = 0.1mA$$

$$\Delta V_{CE} = 5V$$

$$\Delta i_C = 5mA$$



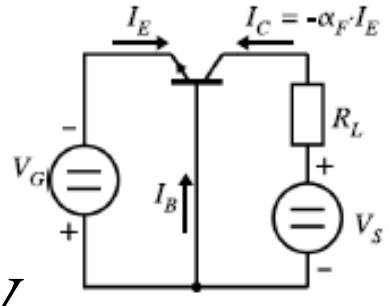
(a) Base characteristics



(b) Collector characteristics

$$V_{CE} = V_S - R_L i_C$$

Base Comune

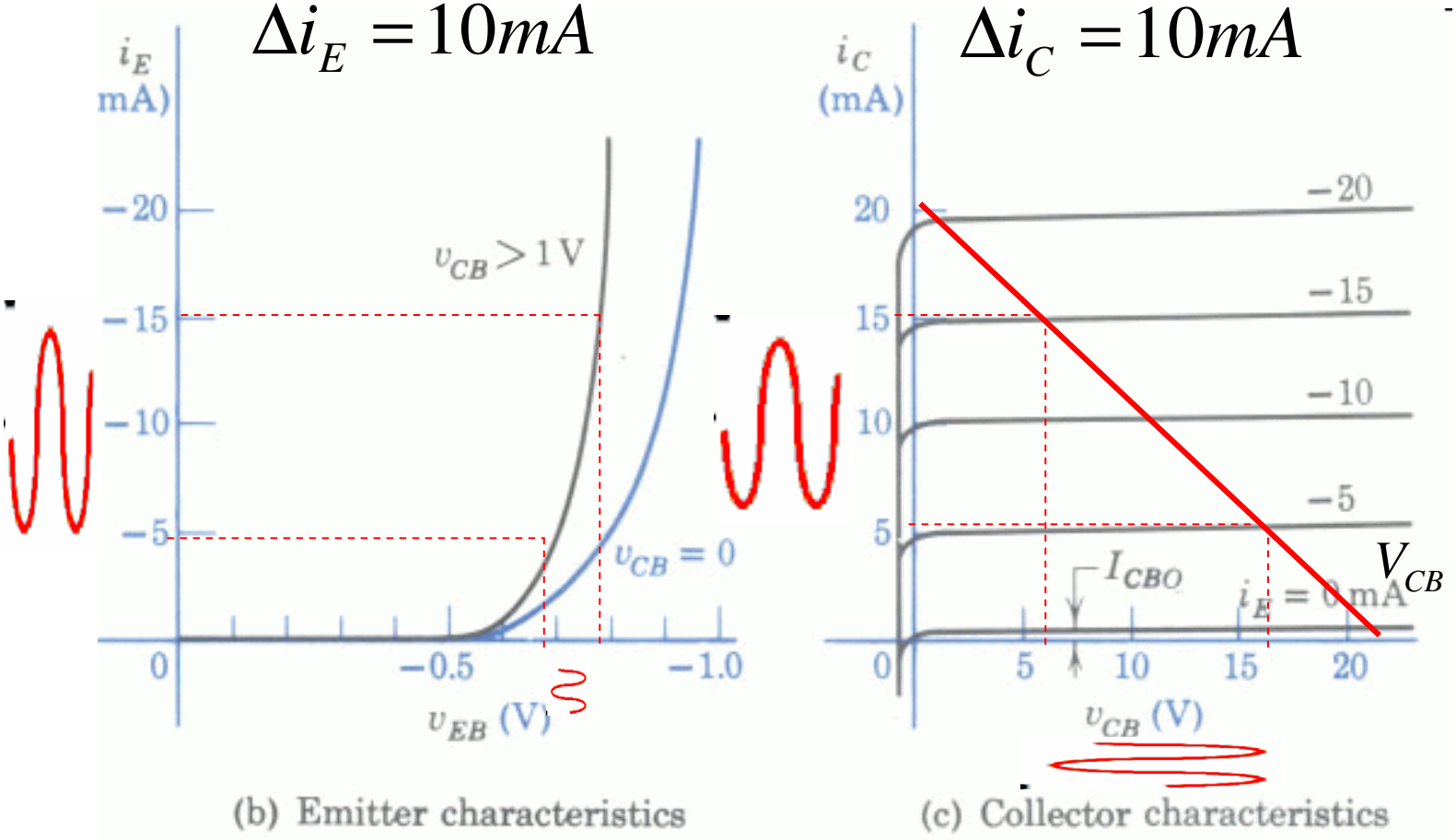


$$\Delta V_{EB} = 0.1V$$

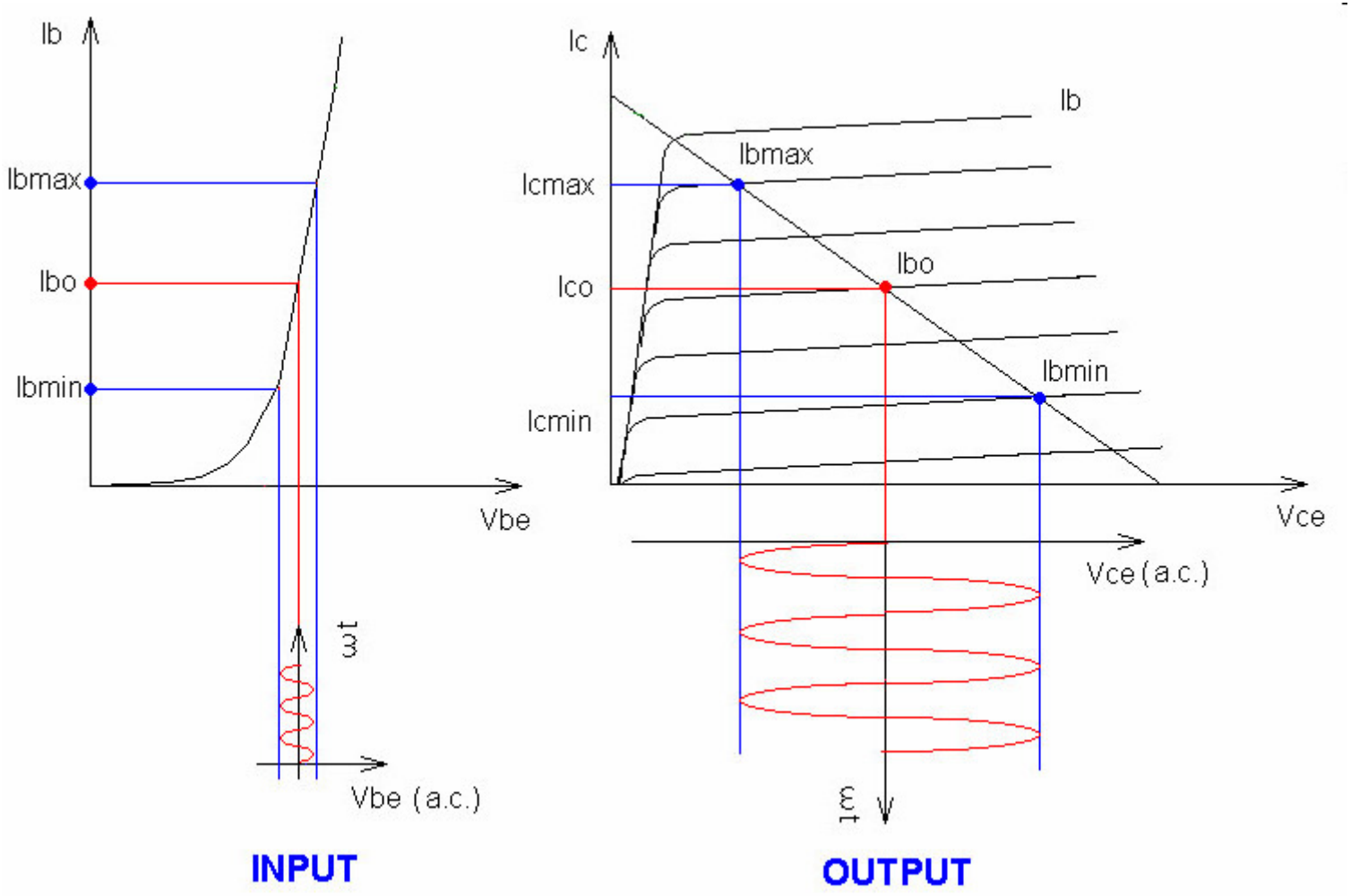
$$\Delta i_E = 10mA$$

$$\Delta V_{CB} = 11V$$

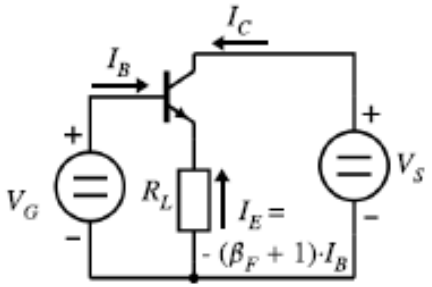
$$\Delta i_C = 10mA$$



$$V_{CB} = V_S - R_L i_C$$


Ib
Ibmax
Ibo
Ibmin
Vbe
ωt
Vbe (a.c.)
INPUT
Ic
Ib
Ibmax
Icmax
Ibo
Ico
Ibmin
Icmin
Vce
Vce (a.c.)
ωt
OUTPUT

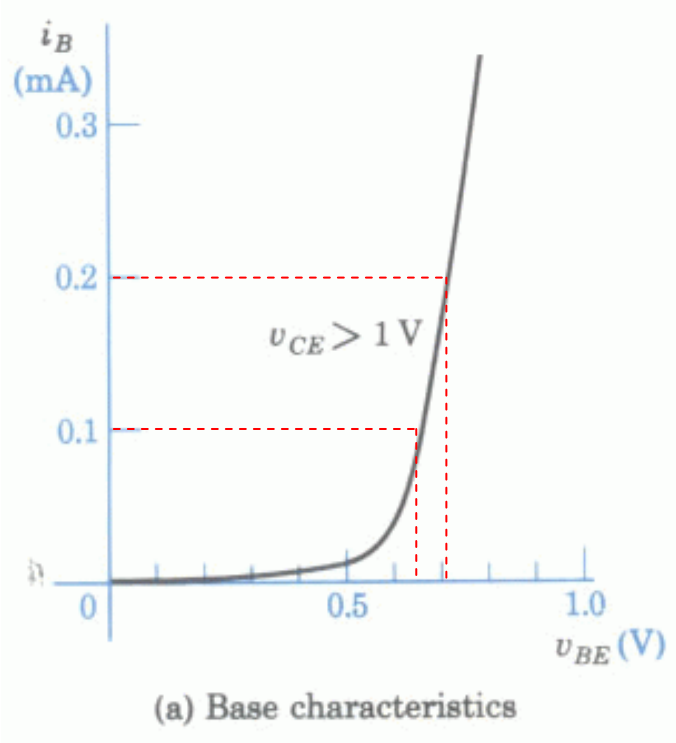
Collettore Comune



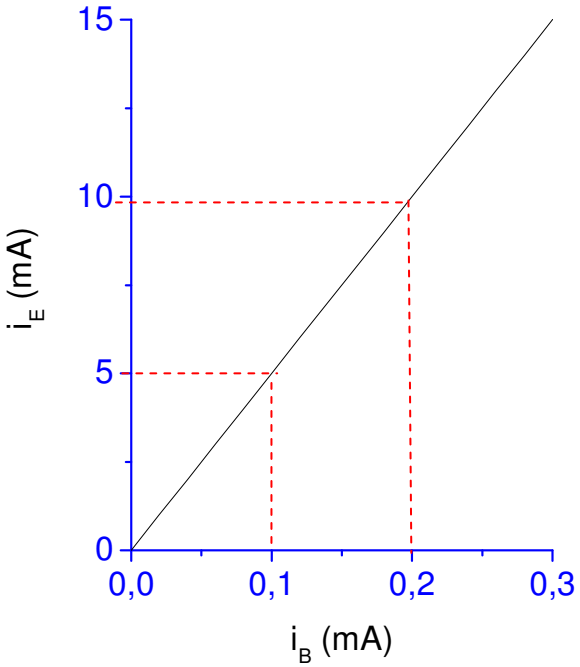
$$\Delta V_{BE} = 0.07V$$

$$\Delta i_B = 0.1mA$$

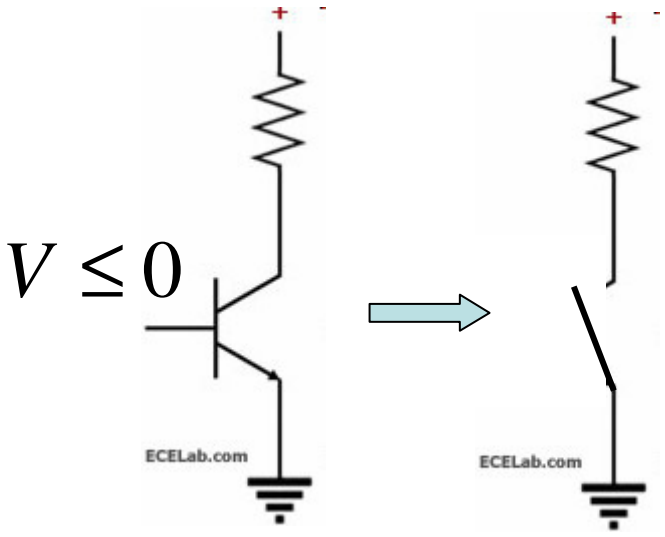
$$\Delta i_E = 5mA$$

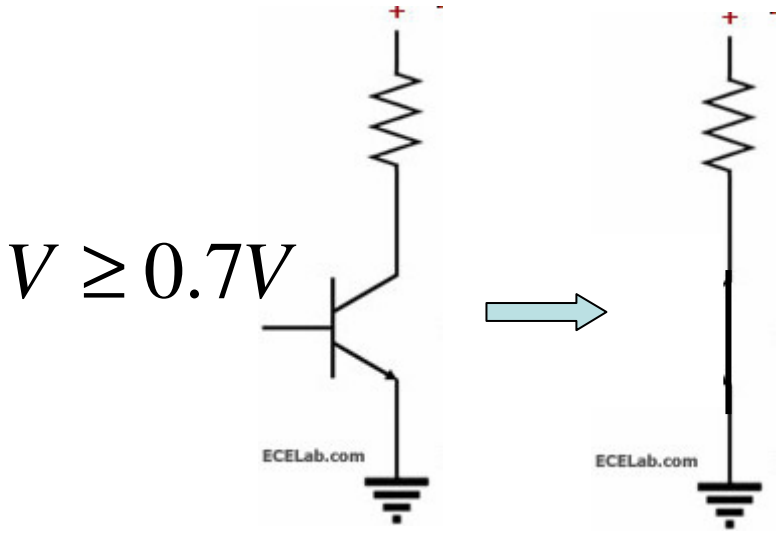


(a) Base characteristics

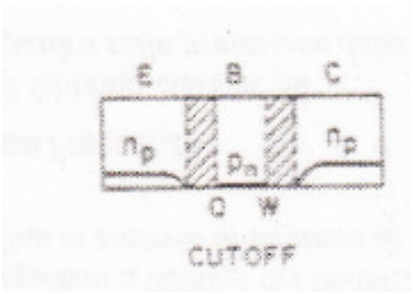


Switch

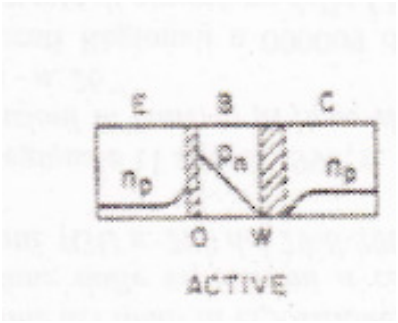




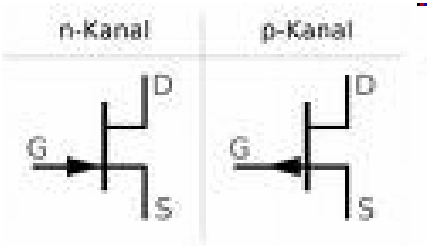
OFF



ON



JFET



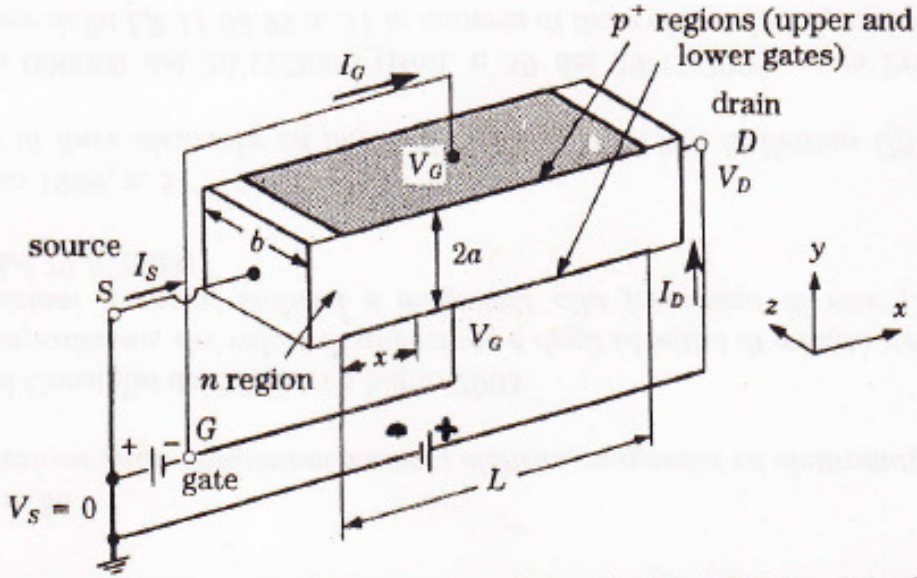


Fig. 10.23. Perspective view of the active part of a junction field-effect transistor. (After Millman and Halkias, "Integrated Electronics: Analog and Digital Circuits and Systems," McGraw–Hill, 1972.)

JFET

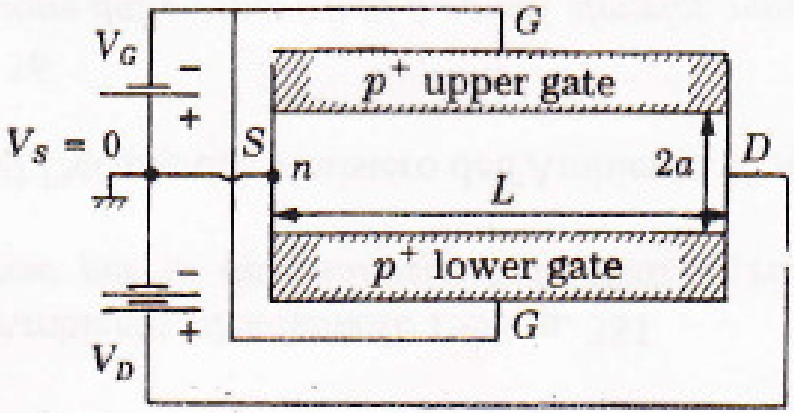


Fig. 10.24. Schematic view of the same transistor showing the doping of various regions. (After Leturcq and Rey, "Physique des Composants Actifs à Semi-conducteurs," Dunod, 1978.)

$$V_G \leq 0 \quad V_D \geq 0$$

JFET

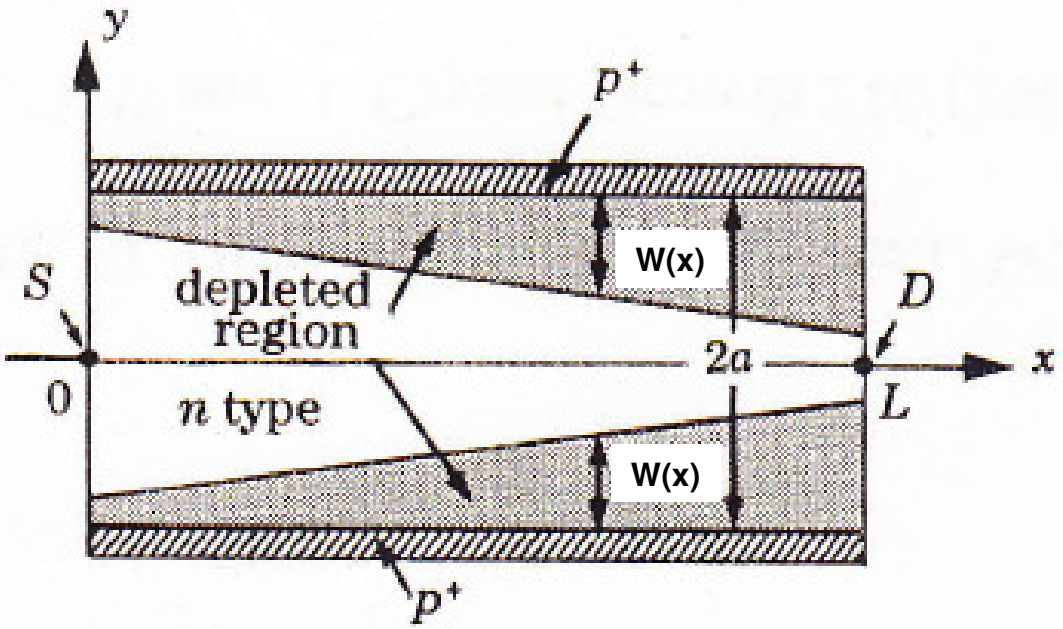


Fig. 10.26. Depleted regions and the conducting channel in a polarized JFET.

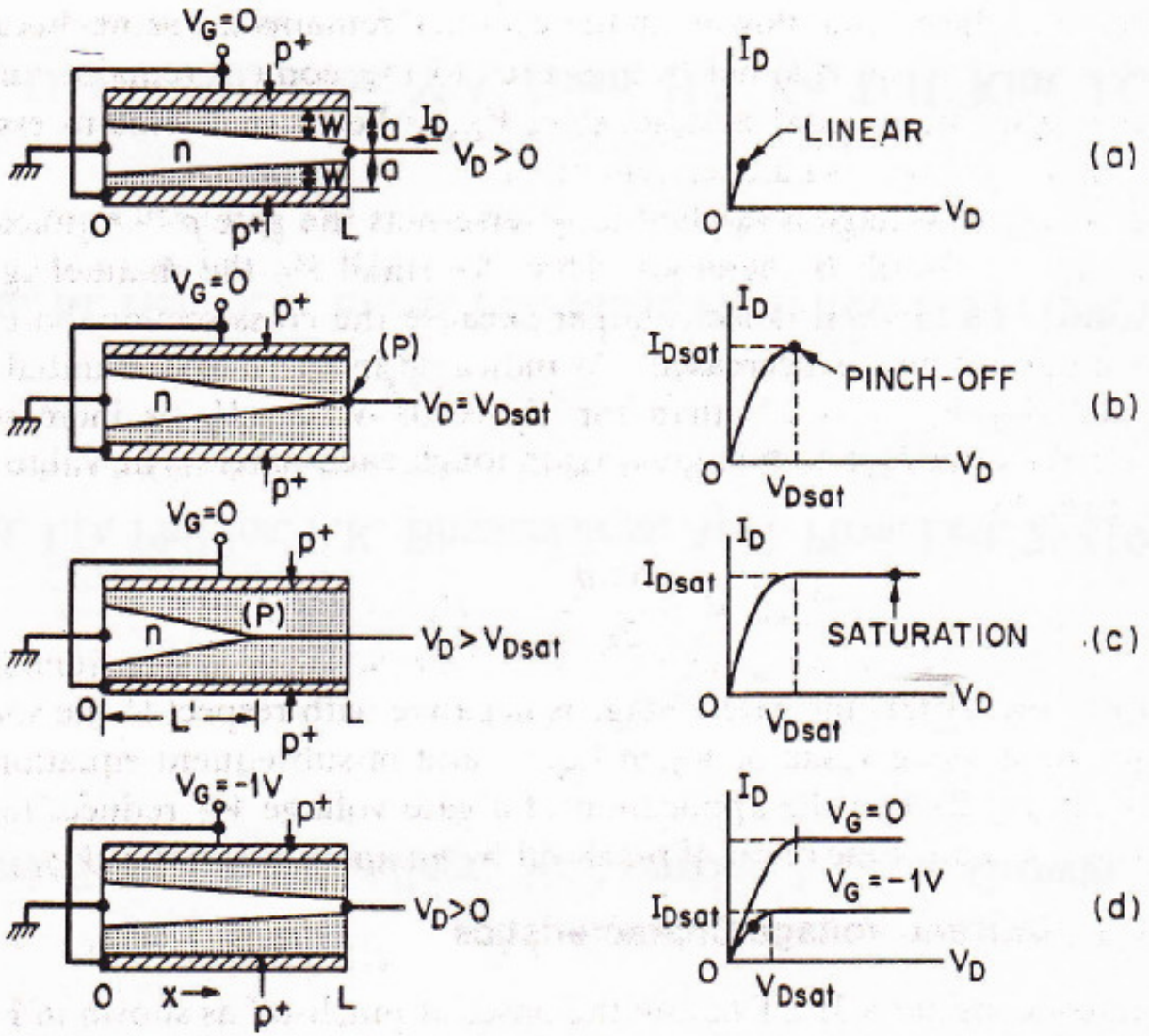
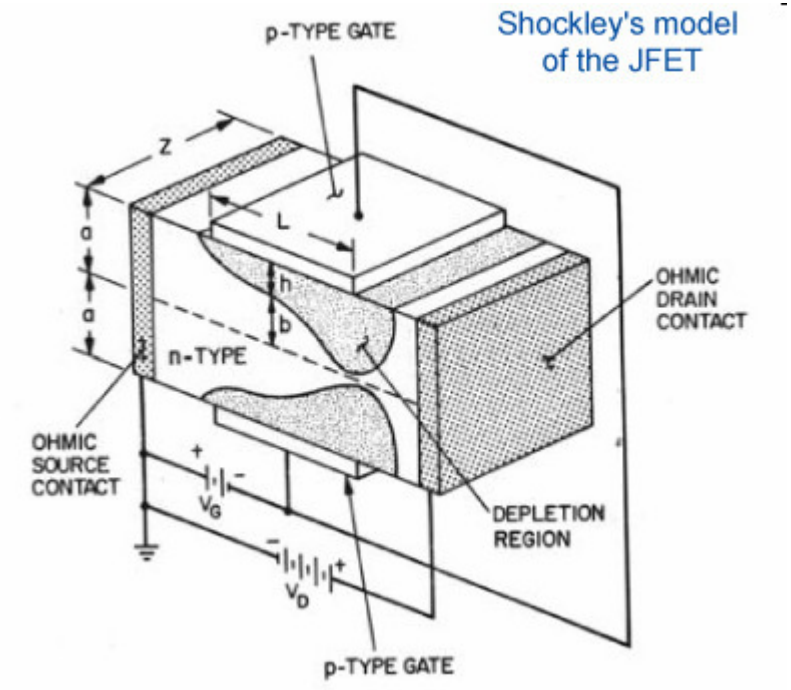


Fig. 10 Variation of depletion layer width and output characteristics of a JFET under various biasing conditions. (*a*) $V_G = 0$ and small V_D. (*b*) $V_G = 0$ and at pinch-off. (*c*) $V_G = 0$ and post pinch-off ($V_D > V_{Dsat}$). (*d*) $V_G = -1$ V and small V_D.

JFET: pinch off



JFET: caratteristiche statiche

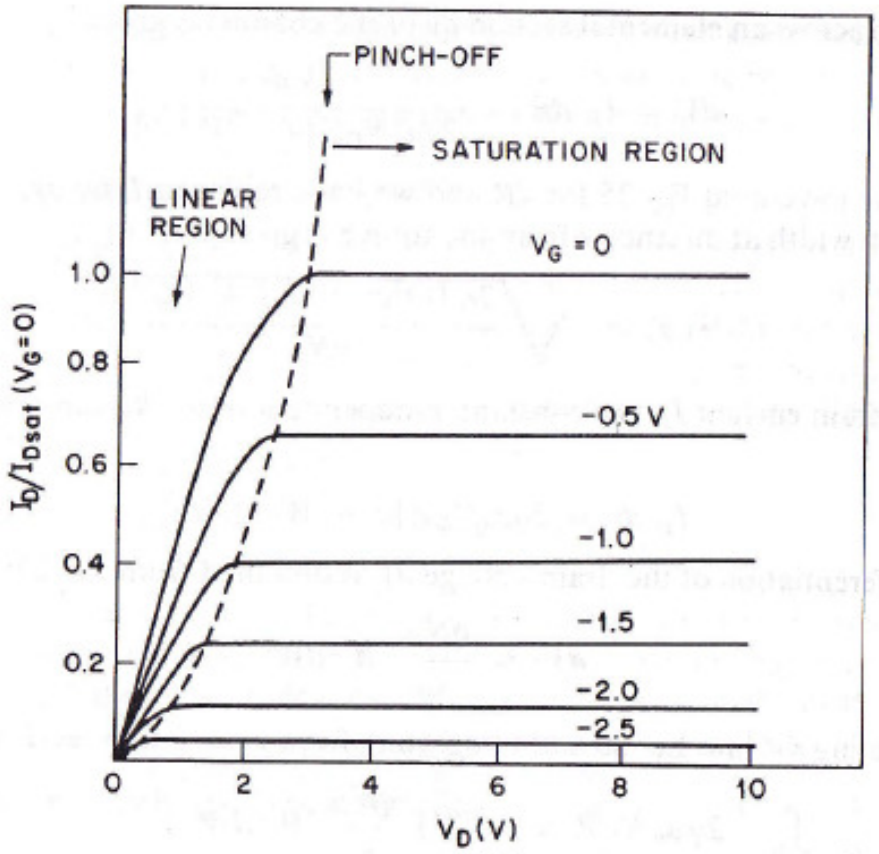


Fig. 12 Normalized ideal current–voltage characteristics with $V_P = 3.2$ V.

JFET: confronto modello dati

$$g_D = \frac{\partial I_D}{\partial V_D}$$ Conduttanza

$$g_m = \frac{\partial I_D}{\partial V_G}$$ Transconduttanza

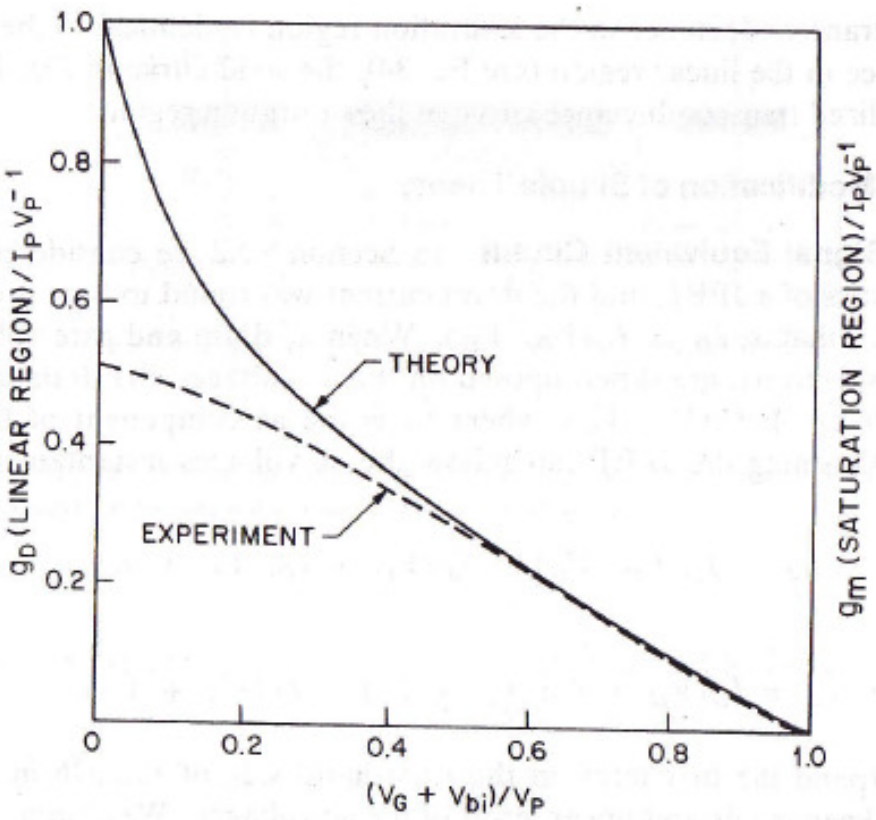


Fig. 13 Normalized drain conductance in the linear region and normalized transconductance in the saturation region versus normalized gate voltage. Solid line is for the ideal case; dotted line is for a practical device having series resistances.

JFET: comportamento dinamico

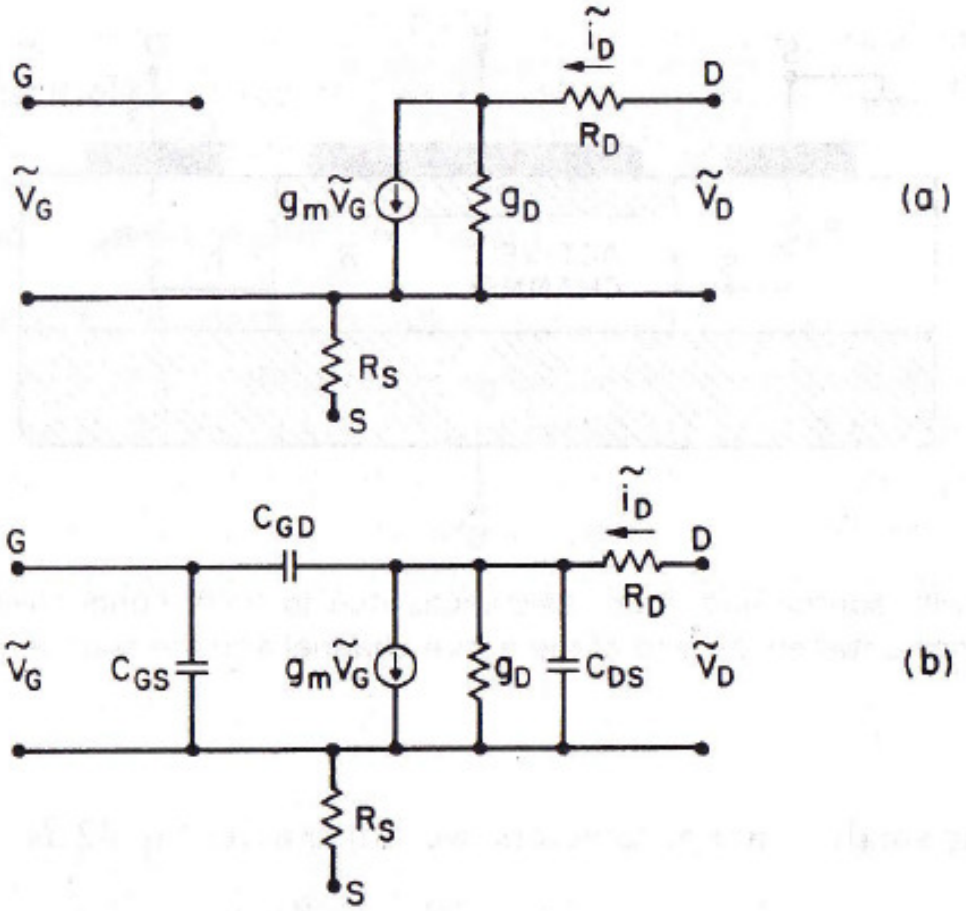


Fig. 15 (*a*) Low-frequency, small-signal equivalent circuit of the JFET. (*b*) High-frequency, small-signal equivalent circuit of the JFET.